MJ13333

Designer's™ Data Sheet

SWITCHMODE Series NPN Silicon Power Transistor

20 AMPERE NPN SILICON POWER TRANSISTORS 400–500 VOLTS 175 WATTS

The MJ13333 transistor is designed for high voltage, high–speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

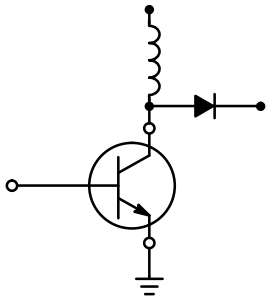
Fast Turn Off Times

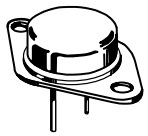
200 ns Inductive Fall Time — 25°C (Typ)
1.8 µs Inductive Storage Time — 25°C (Typ)

Operating Temperature Range –65 to +200°C

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents





CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	400	Vdc
Collector–Emitter voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤10%.
Similar device types available with lower V_{CEO} ratings, see the MJ13330 (200 V) and MJ13331 (250 V).

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	60	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 20 Adc, I_B = 6.7 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 1.8 5.0 2.4	Vdc
Base Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 1.8 1.8	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	125	—	500	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 10 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.02	0.1	μs
Rise Time		t_r	—	0.3	0.7	μs
Storage Time		t_s	—	1.6	4.0	μs
Fall Time		t_f	—	0.3	0.7	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	2.5	5.0	μs
Crossover Time		t_c	—	0.8	2.0	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	1.8	—	μs
Crossover Time		t_c	—	0.4	—	μs
Fall Time		t_{fi}	—	0.2	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

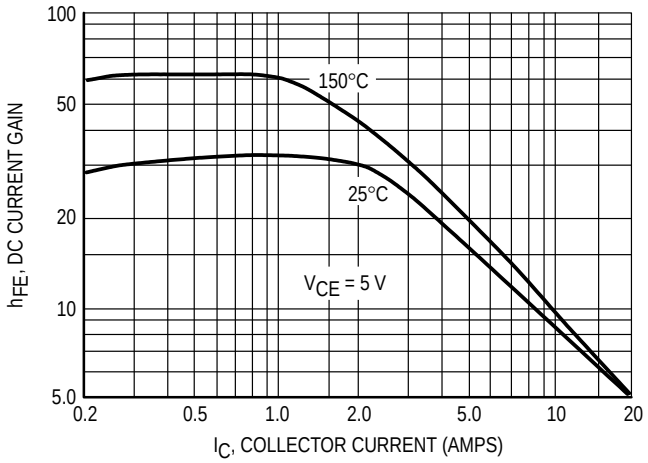


Figure 1. DC Current Gain

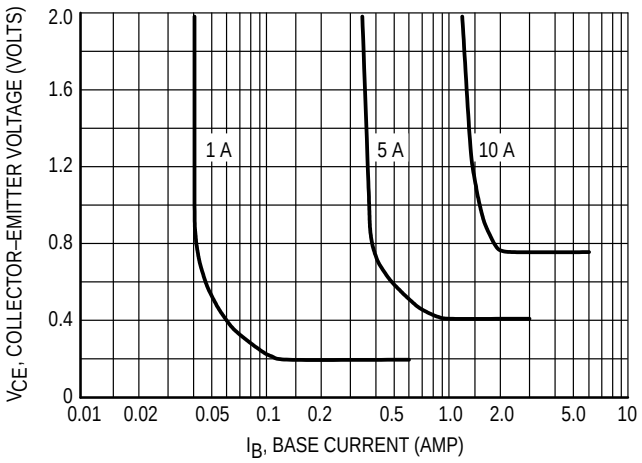


Figure 2. Collector Saturation Region

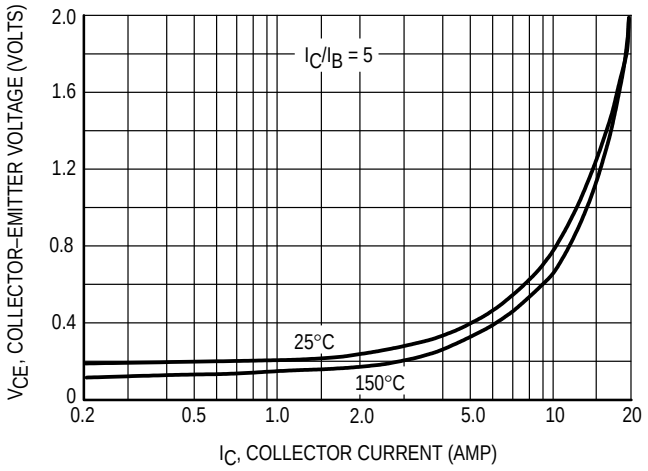


Figure 3. Collector–Emitter Saturation Region

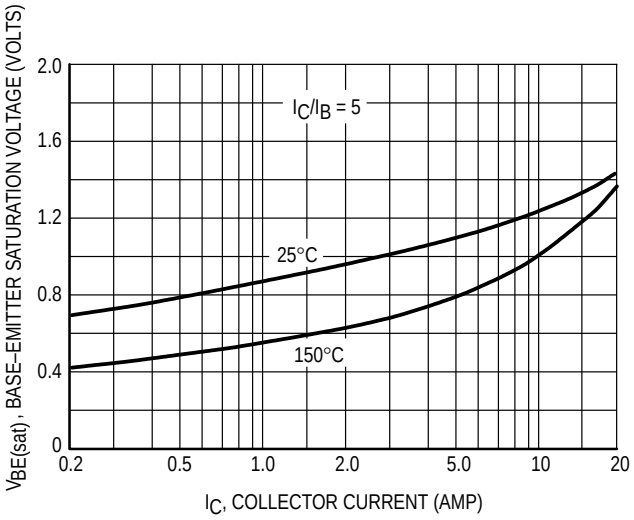


Figure 4. Base–Emitter Voltage

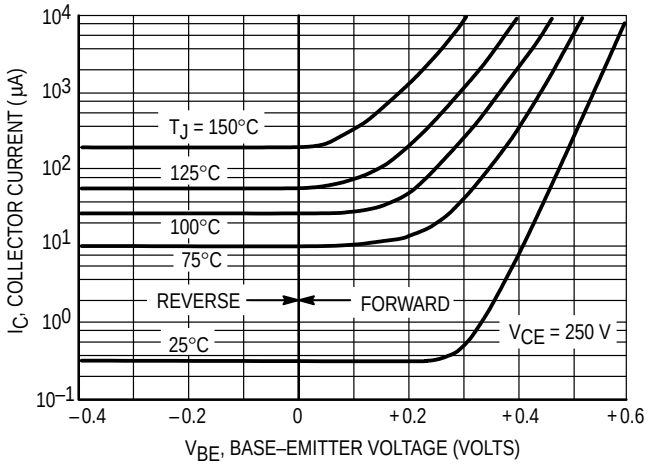


Figure 5. Collector Cutoff Region

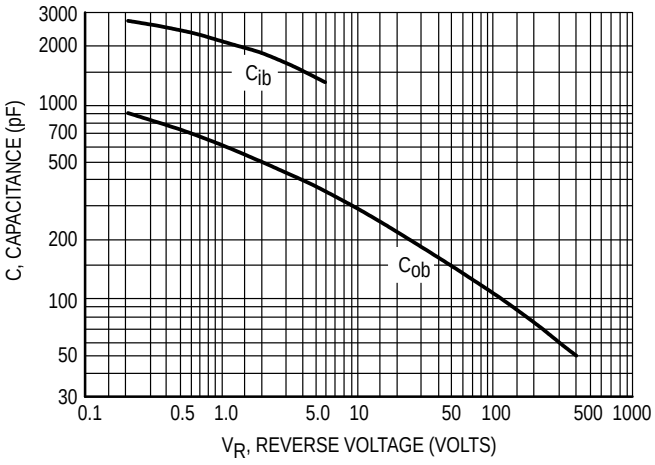


Figure 6. Capacitance

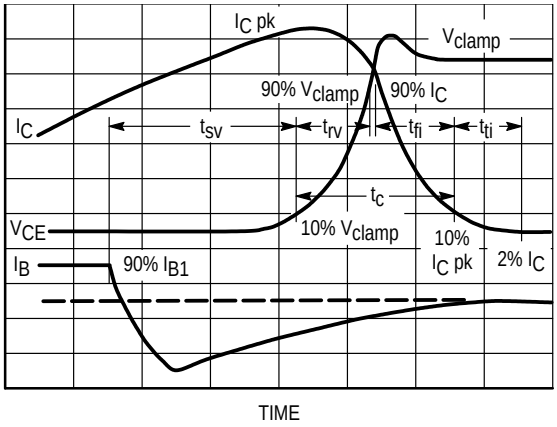


Figure 7. Inductive Switching Measurements

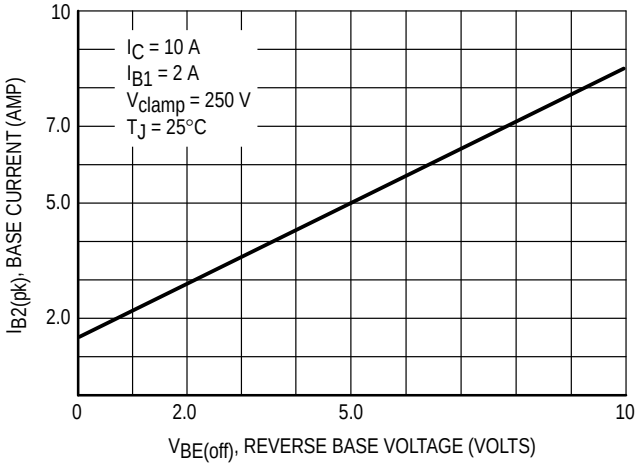


Figure 8. Reverse Base Current versus $V_{BE(off)}$ With No External Base Resistance

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10 – 90% V_{clamp}
t_{fi} = Current Fall Time, 90 – 10% I_C
t_{ti} = Current Tail, 10 – 2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers, However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

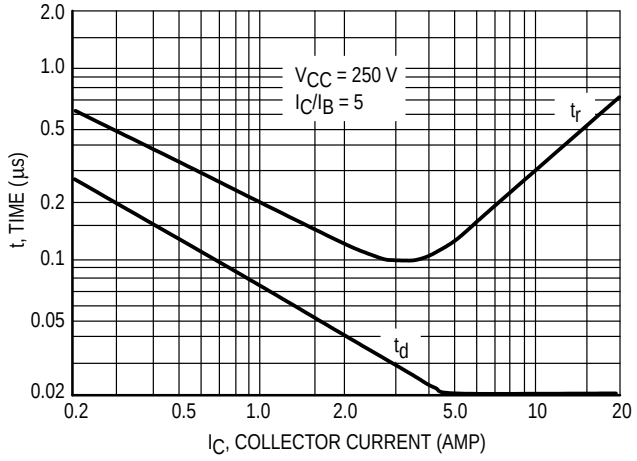


Figure 9. Turn–On Switching Times

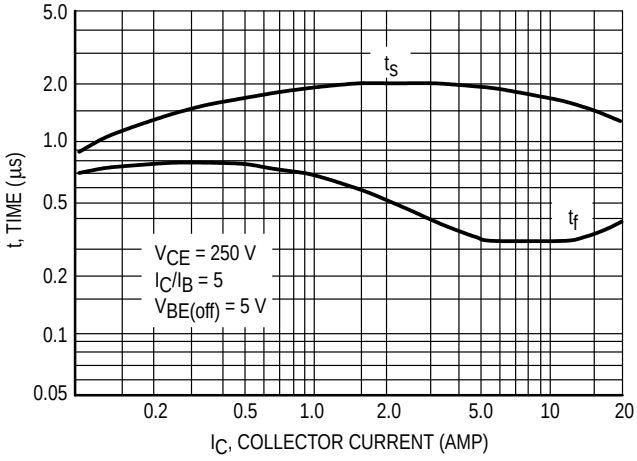


Figure 10. Turn–Off Switching Times

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 1, 0, 2 PW Varied to Attain I_C = 100 mA	250 µF, 470 Ω 2 W, 47 Ω, R1, +15 V, 15 V, 0, 330 Ω, 5.1 Ω 5 W, R2, 50 Ω, 100 Ω, 430 Ω, 39 Ω, 250 µF, –5.2 All Diodes — 1N4934 All NPN — MJE200 All PNP — MJE210 Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	**TURN–ON TIME** I_{B1} I_{B1} adjusted to obtain the forced h_{FE} desired **TURN–OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 10 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT** TUT, 1, INPUT, 2, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, RS = 0.1 Ω SEE ABOVE FOR DETAILED CONDITIONS **OUTPUT WAVEFORMS** I_C, $I_{C(pk)}$, t_f Clamped, t, t_1, t_f, V_{CE}, V_{CE} or V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** TUT, 1, 2, R_L, V_{CC}

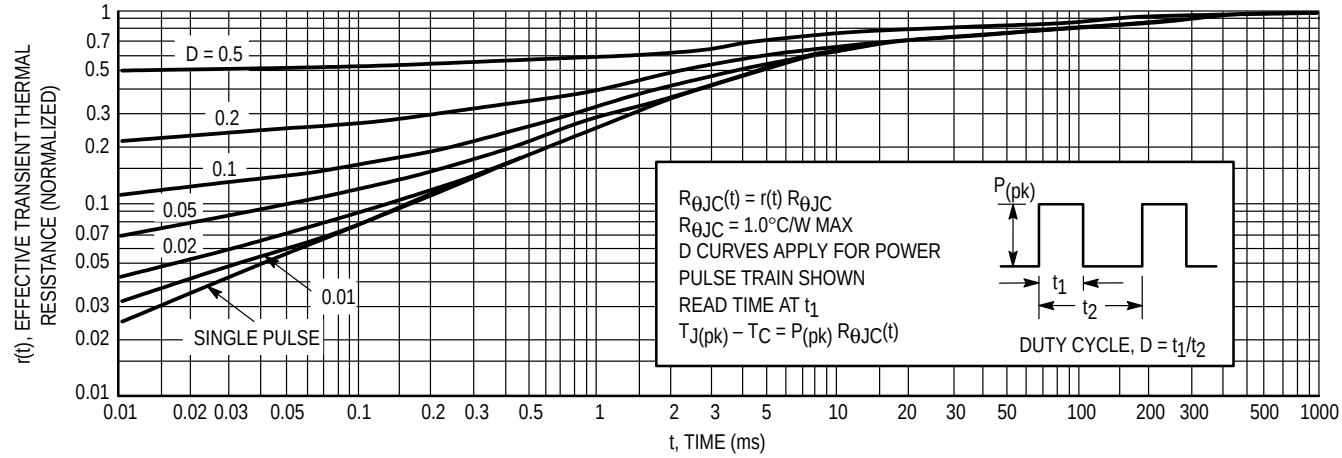


Figure 11. Thermal Response

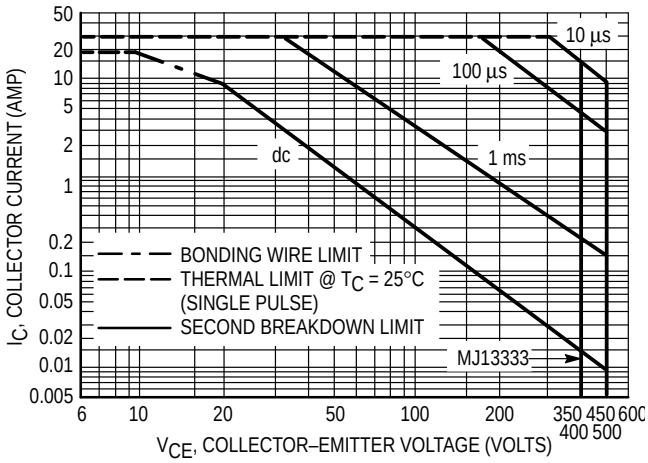


Figure 12. Forward Bias Safe Operating Area

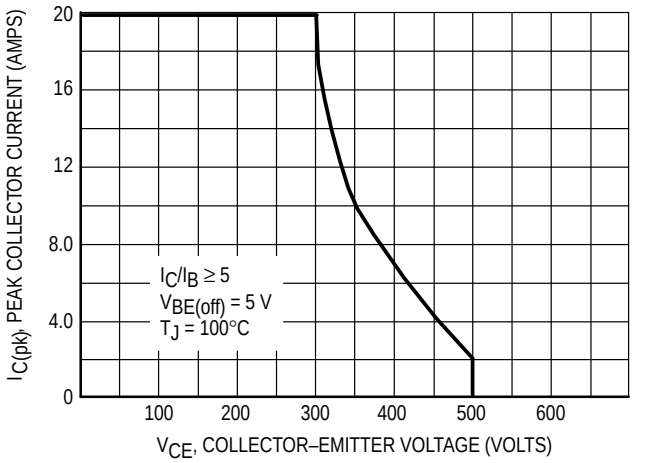


Figure 13. RBSOA, Reverse Bias Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$. $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

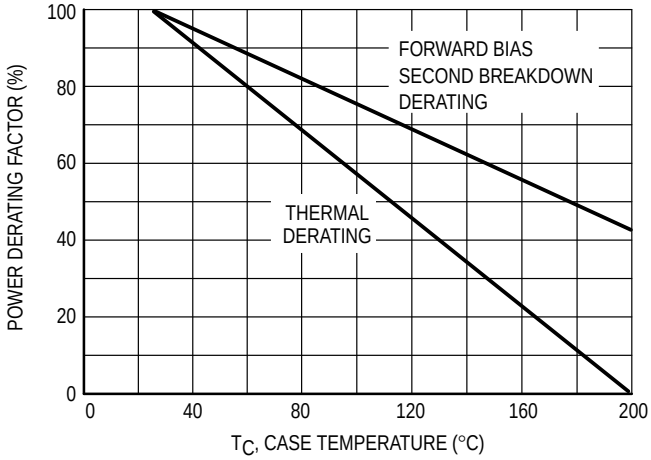
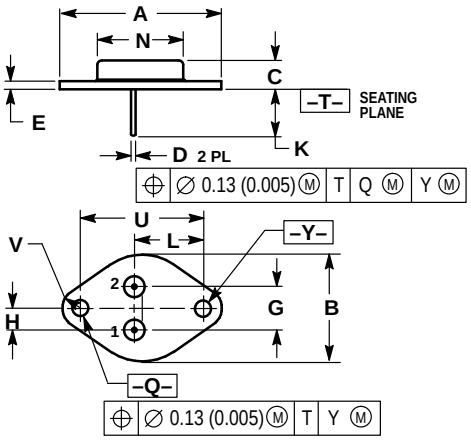


Figure 14. Power Derating

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

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