

High-Frequency N-P-N Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz

March 1993

Features

- Gain-Bandwidth Product (f_T) > 3GHz
- Five Transistors on a Common Substrate

Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations-RF/Mixer/Oscillator
- IF Converter
- IF Amplifiers
- Sense Amplifiers
- Synthesizers
- Synchronous Detectors
- Cascade Amplifiers

Description

The CA3227 and CA3246* consist of five general purpose silicon n-p-n transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3GHz, making them useful from DC to 1.5GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

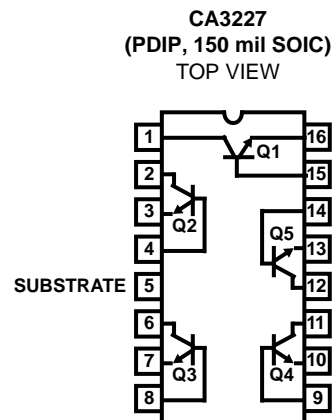
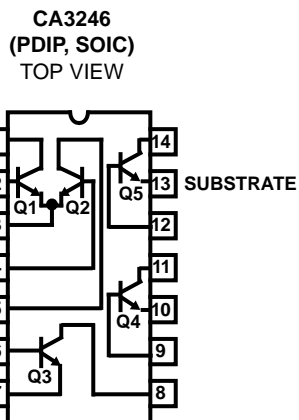
* Formerly RCA Development Nos. TA10854 and TA10855, respectively.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3227E	-55°C to +125°C	16 Lead Plastic DIP
CA3227M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3227M96	-55°C to +125°C	16 Lead Narrow Body SOIC *
CA3246E	-55°C to +125°C	14 Lead Plastic DIP
CA3246M	-55°C to +125°C	14 Lead SOIC
CA3246M96	-55°C to +125°C	14 Lead SOIC *

* Denotes Tape and Reel

Pinouts



Specifications CA3227, CA3246

Absolute Maximum Ratings (T_A = +25°C)

Power Dissipation, P_D:
 Any one transistor 85mW
 Total Package:
 For T_A Up To +75°C 425mW
 For T_A > +75°C Derate Linearly at 6.67mW/°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CE0}) 8V
 Collector-to-Base Voltage (V_{CBO}) 12V
 Collector-to-Substrate Voltage (V_{CIO}) (Note 1) 20V
 Collector Current (I_C) 20mA
 Junction Temperature +175°C
 Junction Temperature (Plastic Package) +150°C
 Lead Temperature (Soldering 10 Sec.) +300°C

Operating Conditions

Operating Temperature Range -55°C ≤ T_A ≤ +125°C
 Storage Temperature Range -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
FOR EACH TRANSISTOR							
Collector-to-Base Breakdown Voltage	V _{(BR)CBO}	I _C = 10μA, I _E = 0	12	20	-	V	
Collector-to-Emitter Breakdown Voltage	V _{(BR)CEO}	I _C = 1mA, I _B = 0	8	10	-	V	
Collector-to-Substrate Breakdown Voltage	V _{(BR)CIO}	I _{C1} = 10μA, I _B = 0, I _E = 0	20	-	-	V	
Emitter-Cutoff-Current (Note 2)	I _{EBO}	V _{EB} = 4.5V, I _C = 0	-	-	10	μA	
Collector-Cutoff-Current	I _{CEO}	V _{CE} = 5V, I _B = 0	-	-	1	μA	
Collector-Cutoff-Current	I _{CBO}	V _{CB} = 8V, I _E = 0	-	-	100	nA	
DC Forward-Current Transfer Ratio	h _{FE}	V _{CE} = 6V	I _C = 10mA	-	110	-	
			I _C = 1mA	40	150	-	
			I _C = 0.1mA	-	150	-	
Base-to-Emitter Voltage	V _{BE}	V _{CE} = 6V, I _C = 1mA	0.62	0.71	0.82	V	
Collector-to-Emitter Saturation Voltage	V _{CE SAT}	I _C = 10mA, I _B = 1mA	-	0.13	0.50	V	
Base-to-Emitter Saturation Voltage	V _{BE SAT}	I _C = 10mA, I _B = 1mA	0.74	-	0.94	V	

NOTES:

- The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (terminal 5/CA3227 and terminal 13/CA3246) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
- On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the h_{FE}. Hence, the use of I_{EBO} rather than V_{(BR)EBO}. These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.

Specifications CA3227, CA3246

Dynamic Electrical Specifications $T_A = +25^\circ\text{C}$, 200MHz, Common Emitter, Typical Values Intended Only for Design Guidance

PARAMETER	SYMBOL	TEST CONDITION	TYPICAL VALUES	UNITS
FOR EACH TRANSISTOR				
Input Admittance	Y_{11} b_{11} ----- g_{11}	$I_C = 1\text{mA}, V_{CE} = 5\text{V}$	4	mmho
			0.75	mmho
Output Admittance	Y_{22} b_{22} ----- g_{22}	$I_C = 1\text{mA}, V_{CE} = 5\text{V}$	2.7	mmho
			0.13	mmho
Forward Transfer Admittance	Y_{21} Y_{21} ----- θ_{21}	$I_C = 1\text{mA}, V_{CE} = 5\text{V}$	29.3	mmho
			-33	degrees
Reverse Transfer Admittance	Y_{12} Y_{12} ----- θ_{12}	$I_C = 1\text{mA}, V_{CE} = 5\text{V}$	0.38	mmho
			-97	degrees
Input Admittance	Y_{11} b_{11} ----- g_{11}	$I_C = 10\text{mA}, V_{CE} = 5\text{V}$	4.8	mmho
			2.85	mmho
Output Admittance	Y_{22} b_{22} ----- g_{22}	$I_C = 10\text{mA}, V_{CE} = 5\text{V}$	2.75	mmho
			0.9	mmho
Forward Transfer Admittance	Y_{21} Y_{21} ----- θ_{21}	$I_C = 10\text{mA}, V_{CE} = 5\text{V}$	95	mmho
			-62	degrees
Reverse Transfer Admittance	Y_{12} Y_{12} ----- θ_{12}	$I_C = 10\text{mA}, V_{CE} = 5\text{V}$	0.39	mmho
			-97	degrees
Small Signal Forward Current Transfer Ratio	h_{21}	$I_C = 1\text{mA}, V_{CE} = 5\text{V}$	7.1	
		$I_C = 10\text{mA}, V_{CE} = 5\text{V}$	17	
TYPICAL CAPACITIES AT 1MHz, THREE-TERMINAL MEASUREMENT				
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 6\text{V}$	0.3	pF
Collector-to-Substrate Capacitance	C_{Cl}	$V_{Cl} = 6\text{V}$	1.6	pF
Collector-to-Emitter Capacitance	C_{CE}	$V_{CE} = 6\text{V}$	0.4	pF
Emitter-to-Base Capacitance	C_{EB}	$V_{EB} = 3\text{V}$	0.75	pF

Spice Model (Spice 2G.6)

.model NPN

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+      BF = 2.610E + 02      BR = 4.401E + 00      IS = 6.930E - 16      RB = 130.0E + 00
+      RC = 1.000E + 01      RE = 7.396E - 01      VA = 6.300E + 01      VB = 2.208E + 00
+      IK = 1.000E - 01      ISE = 1.87E - 14      NE = 1.653E + 00      IKR = 1.000E - 02
+      ISC = 9.25E - 14      NC = 1.333E + 00      TF = 1.775E - 11      TR = 1.000E - 09
+      CJS = 1.800E - 12      CJE = 1.010E - 12      PE = 8.350E - 01      ME = 4.460E - 01
+      CJC = 9.100E - 13      PC = 3.850E - 01      MC = 2.740E - 01      KF = 0.000E + 00
+      AF = 1.000E + 00      EF = 1.000E + 00      FC = 5.000E - 01      PJS = 5.410E - 01
+      MJS = 3.530E - 01      RBM = 30.00      RBV = 100      IRB = 0.00
    
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Please Note: No measurements have been made to model the reverse AC operation (tr is an estimation)

Typical Performance Curves

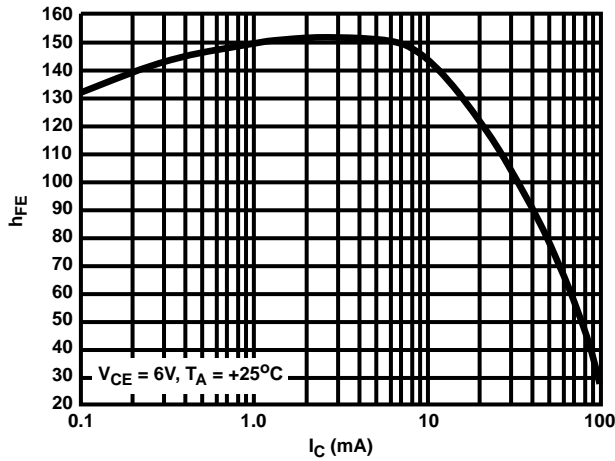


FIGURE 1. h_{FE} vs COLLECTOR CURRENT

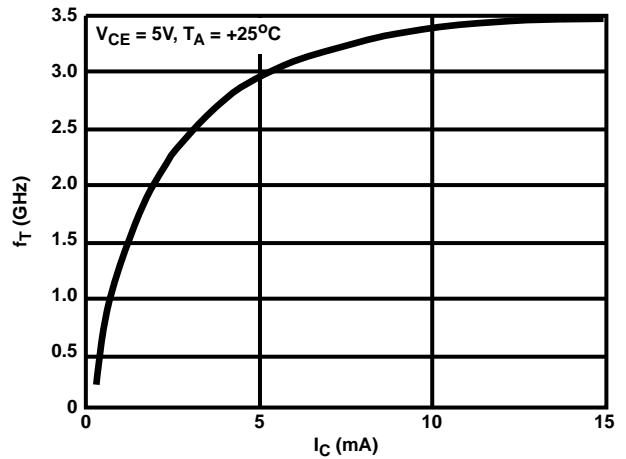


FIGURE 2. f_T vs COLLECTOR CURRENT

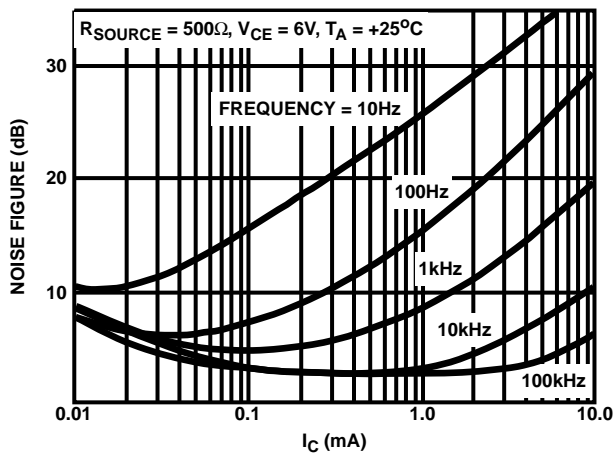


FIGURE 3. NOISE FIGURE vs COLLECTOR CURRENT

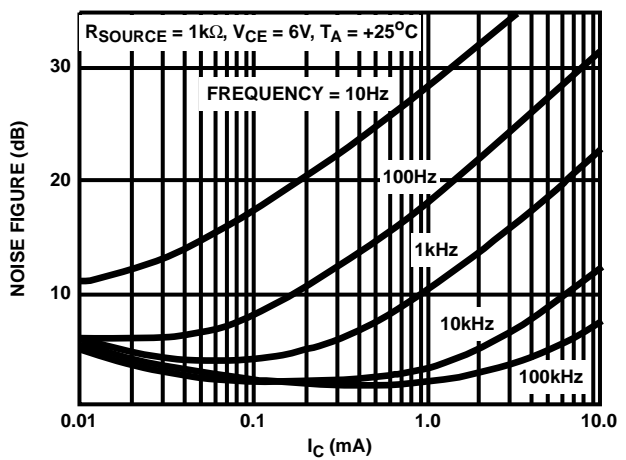


FIGURE 4. NOISE FIGURE vs COLLECTOR CURRENT

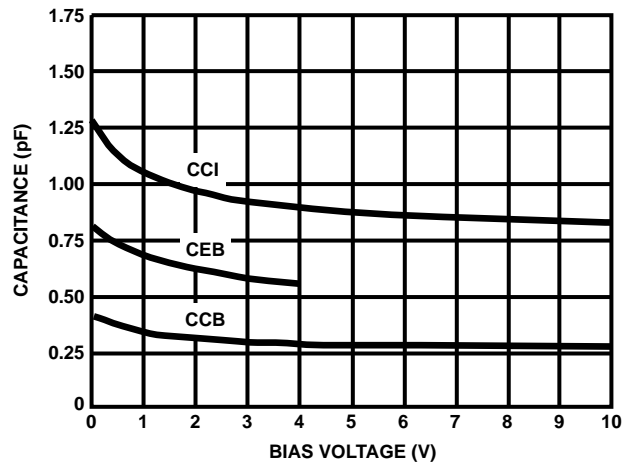


FIGURE 5. CAPACITANCE vs BIAS VOLTAGE

CA3227, CA3246

Die Characteristics

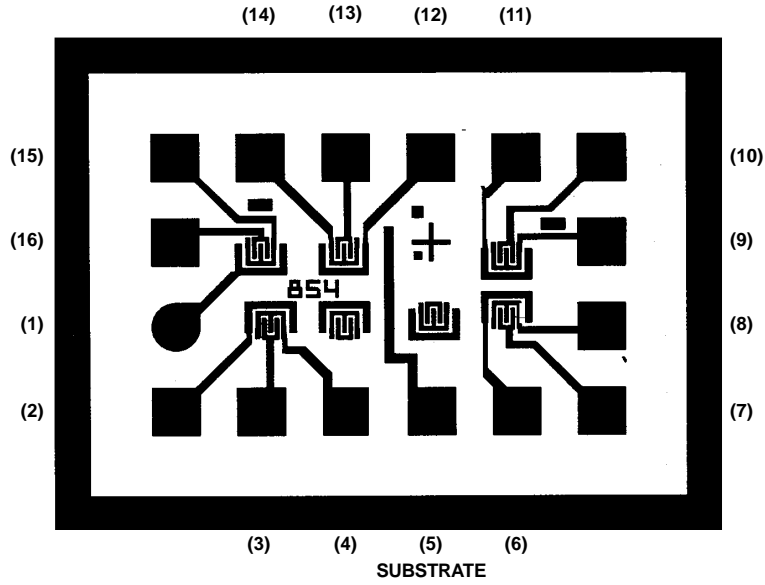
DIE DIMENSIONS:

46 x 32 mils CA3227

47 x 33 mils CA3246

Metallization Mask Layout

CA3227



CA3246

