HARRIS SEMICONDUCTOR

CA3086

General Purpose N-P-N Transistor Array

March 1993

Applications

- **Three Isolated Transistors and One Differentially Connected Transistor Pair For Low-Power Applications from DC to 120 MHz**
- **General-Purpose Use in Signal Processing Systems Operating in the DC to 190MHz Range**
- **Temperature Compensated Amplifiers**
- **See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array"' for Suggested Applications**

Description

The CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

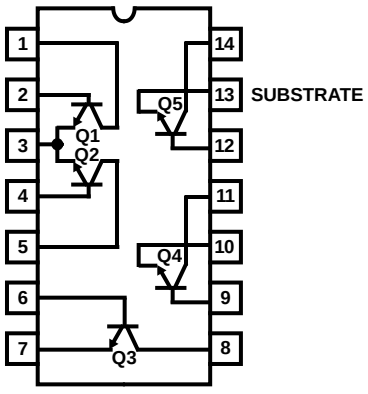
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3086	-55^{o}C to +125^{o}C	14 Lead Plastic DIP
CA3086M	-55^{o}C to +125^{o}C	14 Lead SOIC
CA3086M96	-55^{o}C to +125^{o}C	14 Lead SOIC*
CA3086F	-55^{o}C to +125^{o}C	14 Lead Ceramic DIP

* Denotes Tape and Reel

Pinout

CA3086
(PDIP, CDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **483.2**

Absolute Maximum Ratings

Power Dissipation
- Any one transistor 300mW
- Total package up to T_A = +55°C 750mW
- Above T_A = +55°C. . . . . .Derate linearly 6.67 mW/°C

Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.). . . . . +300°C
The following ratings apply for each transistor in the device:
- Collector-to-Emitter Voltage, V_{CEO} 15V
- Collector-to-Base Voltage, V_{CBO}. 20V
- Collector-to-Substrate Voltage, V_{ClO} (Note 1). 20V
- Emitter-to-Base Voltage, V_{EBO} 5V
- Collector Current, I_C 50mA

Operating Conditions

Ambient Temperature Range
- Operating. . . . . -55°C to +125°C
- Storage . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C, For Equipment Design

PARAMETERS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10µA, I_E = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)ClO}$	I_C = 10µA, I_{CI} = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10µA, I_C = 0	5	7	-	V
Collector-Cutoff Current (Figure 1)	I_{CBO}	V_{CB} = 10V, I_E = 0,	-	0.002	100	nA
Collector-Cutoff Current (Figure 2)	I_{CEO}	V_{CE} = 10V, I_B = 0,	-	(Figure 2)	5	µA
DC Forward-Current Transfer Ratio (Figure 3)	h_{FE}	V_{CE} = 3V, I_C = 1mA	40	100	-	

NOTE:

1. The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

Electrical Specifications T_A = +25°C, Typical Values Intended Only for Design Guidance

PARAMETERS	SYMBOLS	TEST CONDITIONS		TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio (Figure 3)	h_{FE}	V_{CE} = 3V	I_C = 10mA	100	
			I_C = 10µA	54	
Base-to-Emitter Voltage (Figure 4)	V_{BE}	V_{CE} = 3V	I_E = 1 mA	0.715	V
			I_E = 10mA	0.800	V
V_{BE} Temperature Coefficient (Figure 5)	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1 mA		-1.9	mV/°C
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 1mA, I_C = 10mA		0.23	V
Noise Figure (Low Frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100µA, R_S = 1kΩ		3.25	dB

Electrical Specifications $T_A = +25^oC$, Typical Values Intended Only for Design Guidance **(Continued)**

PARAMETERS	SYMBOLS	TEST CONDITIONS	TYPICAL VALUES	UNITS
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:		f = 1kHz, V_{CE} = 3V, I_C = 1mA		
Forward Current-Transfer Ratio (Figure 6)	h_{FE}		100	-
Short-Circuit Input Impedance (Figure 6)	h_{IE}		3.5	kΩ
Open-Circuit Output Impedance (Figure 6)	h_{OE}		15.6	µmho
Open-Circuit Reverse-Voltage Transfer Ratio (Figure 6)	h_{RE}		1.8×10^{-4}	-
Admittance Characteristics:		f = 1MHz, V_{CE} = 3V, I_C = 1mA		
Forward Transfer Admittance (Figure 7)	y_{FE}		31 - j1.5	mmho
Input Admittance (Figure 8)	y_{IE}		0.3 + j0.04	mmho
Output Admittance (Figure 9)	y_{OE}		0.001 + j0.03	mmho
Reverse Transfer Admittance (Figure 10)	y_{RE}		See Figure 10	-
Gain-Bandwidth Product (Figure 11)	f_T	V_{CE} = 3V, I_C = 3mA	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0	0.58	pF
Collector-to-Substrate Capacitance	C_{ClO}	$V_{C\,I}$ = 3V, I_C = 0	2.8	pF

Typical Static Characteristics for Each Transistor

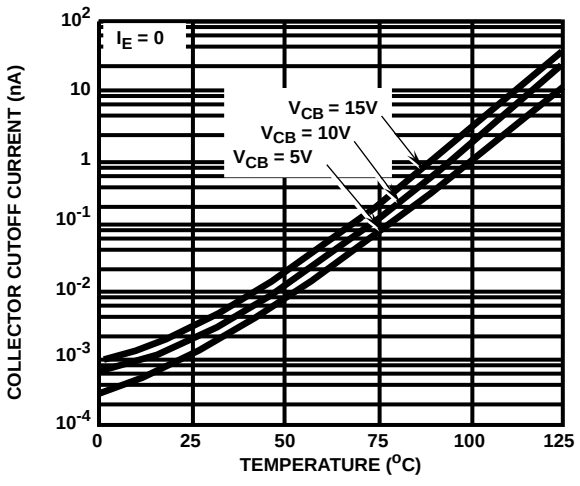


FIGURE 1. I_{CBO} vs TEMPERATURE

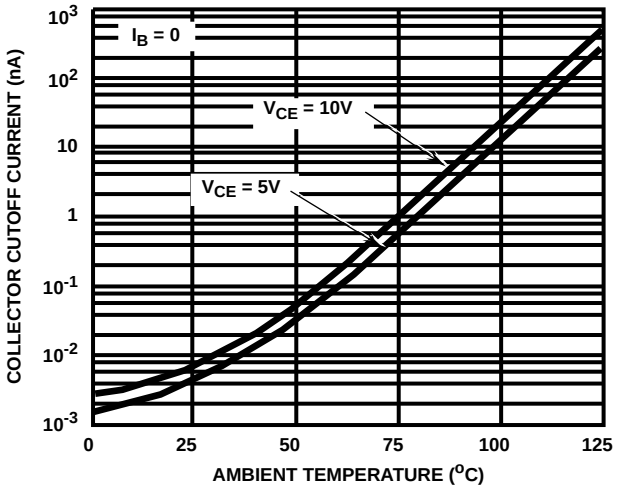


FIGURE 2. I_{CEO} vs TEMPERATURE

Typical Static Characteristics for Each Transistor (Continued)

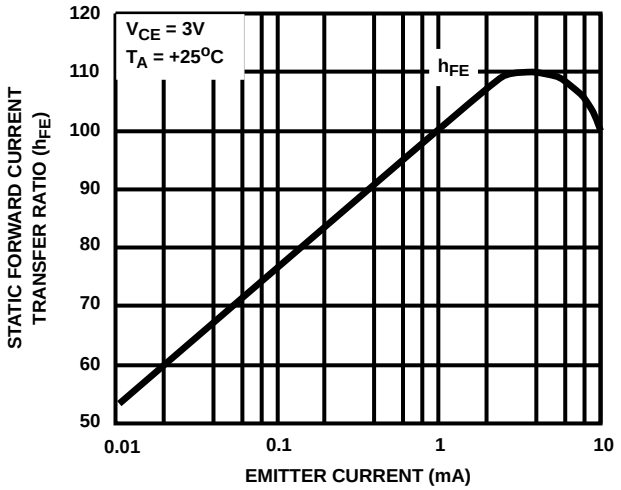


FIGURE 3. h_{FE} vs I_E

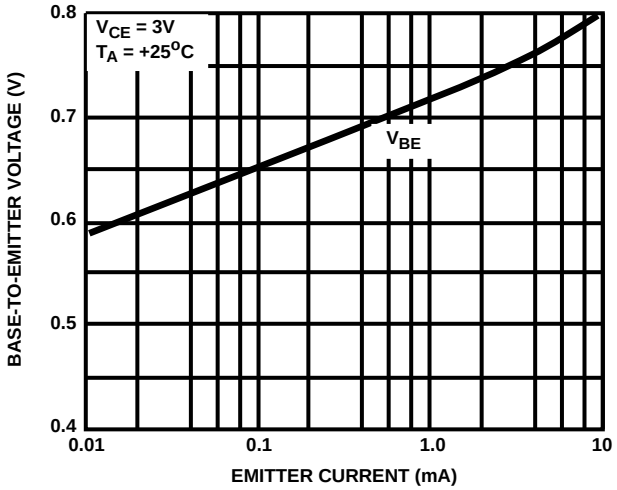


FIGURE 4. V_{BE} vs I_E

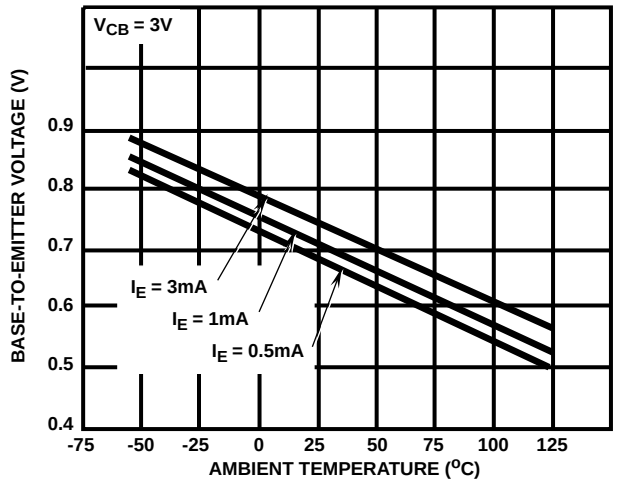


FIGURE 5. V_{BE} vs TEMPERATURE

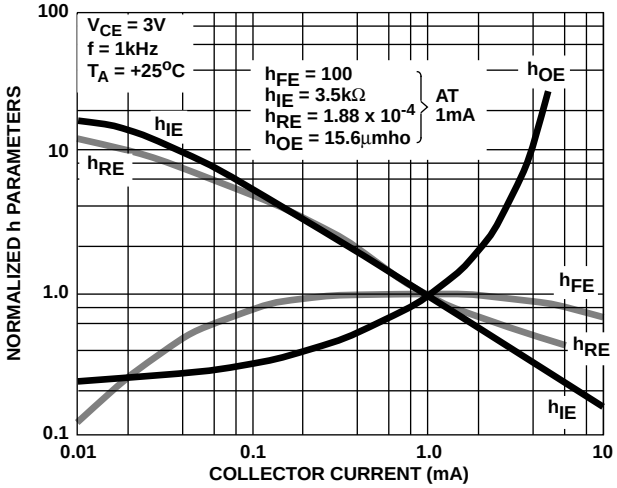


FIGURE 6. NORMALIZED h_{FE}, h_{IE}, h_{RE}, h_{OE} vs I_C

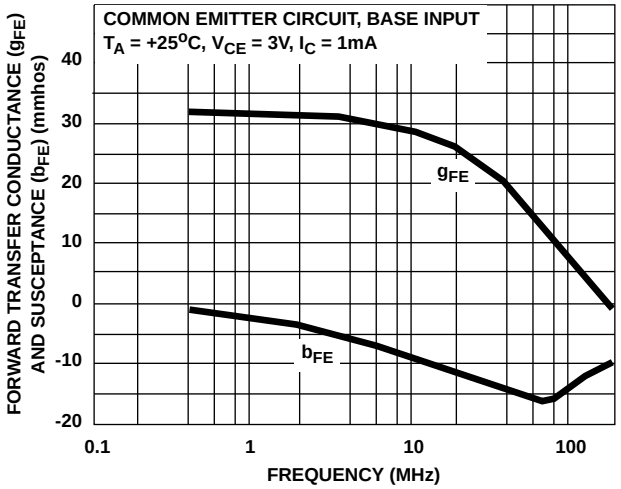


FIGURE 7. y_{FE} vs FREQUENCY

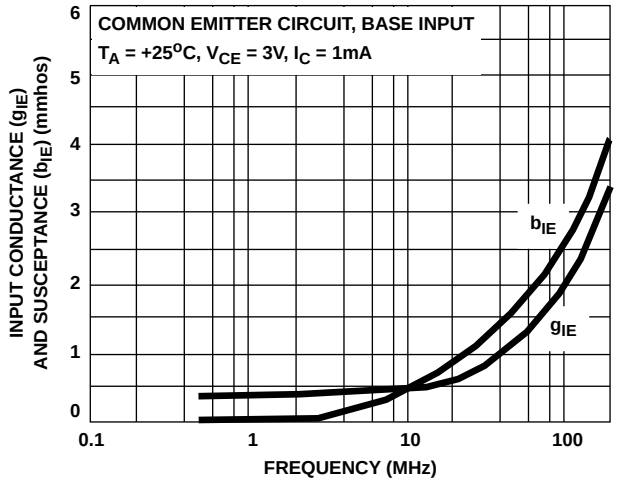


FIGURE 8. y_{IE} vs FREQUENCY

Typical Static Characteristics for Each Transistor (Continued)

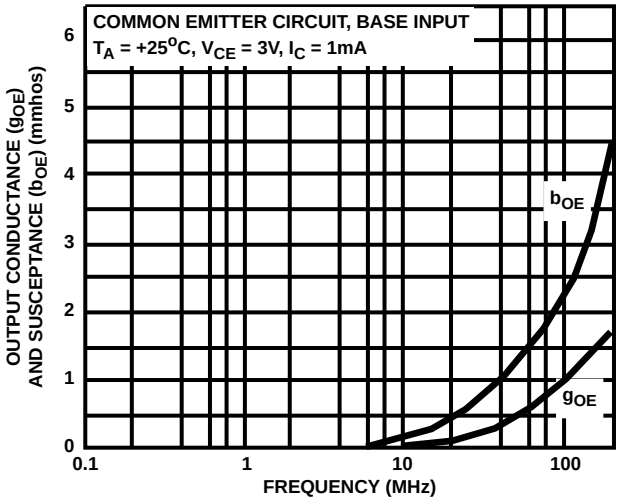


FIGURE 9. y_{OE} vs FREQUENCY

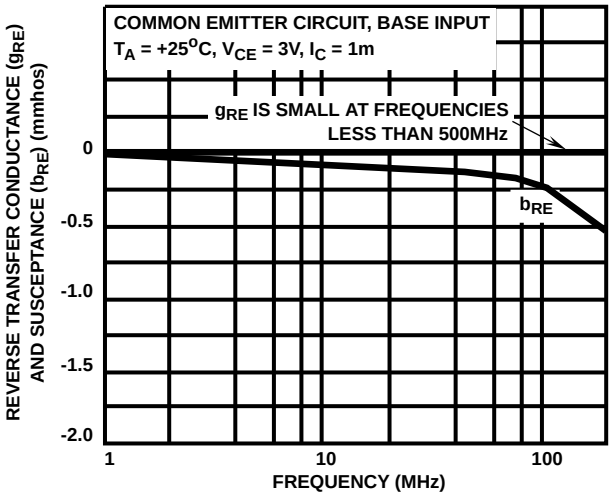


FIGURE 10. y_{RE} vs FREQUENCY

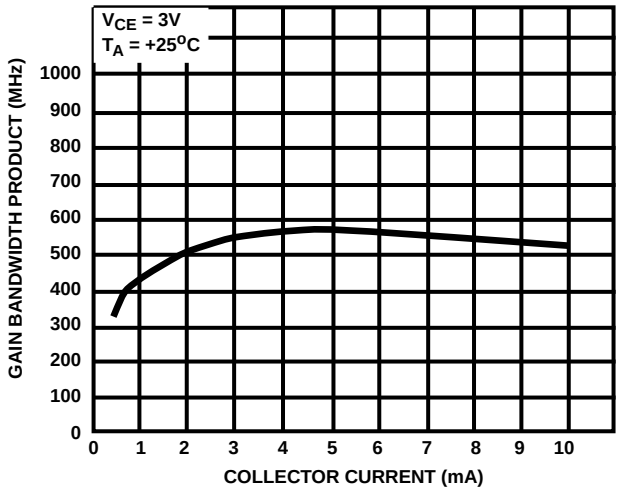


FIGURE 11. f_T vs I_C