

March 1993

Diode Array

Features

- Six Matched Diodes on a Common Substrate
- Excellent Reverse Recovery Time 1ns Typical
- Matched Monolithic Construction
 - V_F Matched Within 5mV
- Low Diode Capacitance
 - $C_D = 0.65\text{pF}$ Typical at $V_R = -2\text{V}$

Applications

- Ultra-Fast Low Capacitance Matched Diodes for Applications in Communications and Switching Systems
- Balanced Modulators or Demodulators
- Ring Modulators
- High Speed Diode Gates
- Analog Switches

Description

The CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

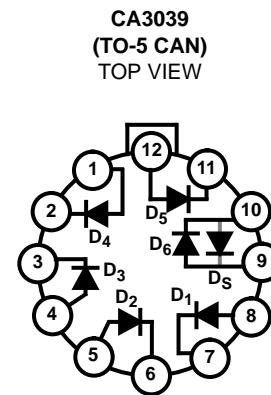
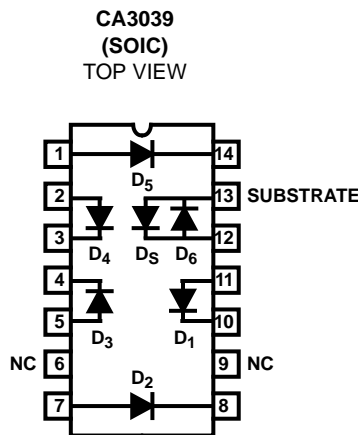
For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3039	-55°C to +125°C	12 Pin CAN
CA3039M	-55°C to +125°C	14 Lead SOIC
CA3039M96	-55°C to +125°C	14 Lead SOIC*

* Denotes Tape and Reel

Pinouts



Typical Performance Curves

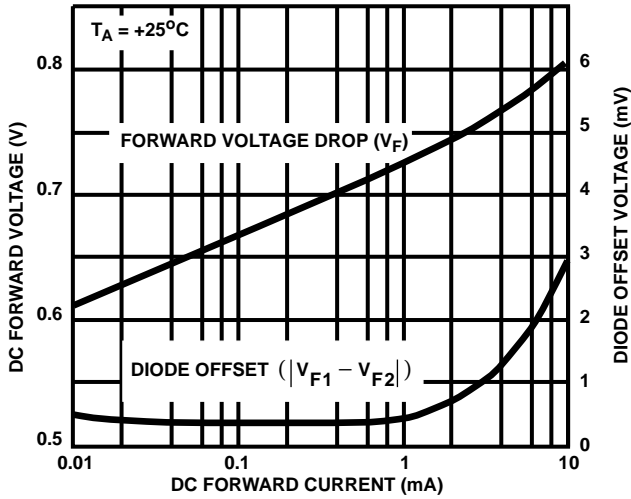


FIGURE 1. DC FORWARD VOLTAGE DROP (ANY DIODE) AND DIODE OFFSET VOLTAGE vs DC FORWARD CURRENT

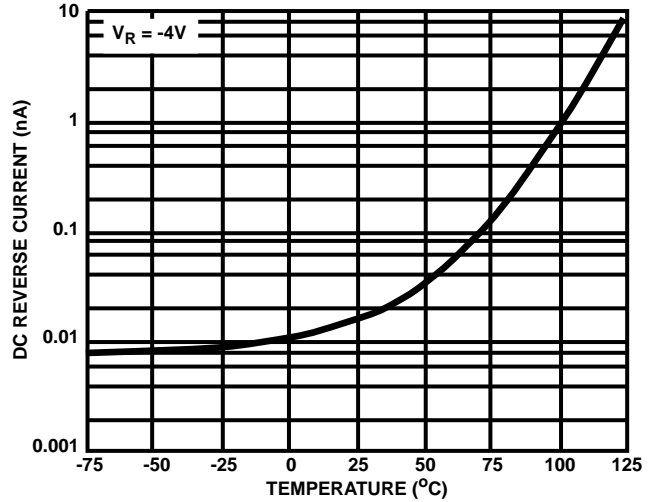


FIGURE 2. DC REVERSE (LEAKAGE) CURRENT (D₁ - D₅) vs TEMPERATURE

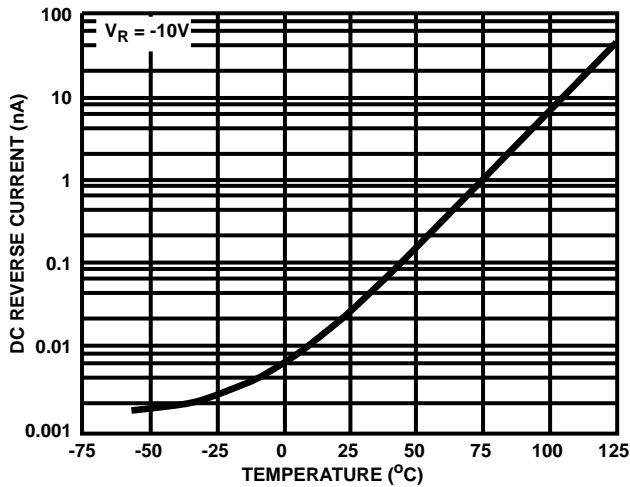


FIGURE 3. DC REVERSE (LEAKAGE) CURRENT BETWEEN D₁, D₂, D₃, D₄, D₅ AND SUBSTRATE vs TEMPERATURE

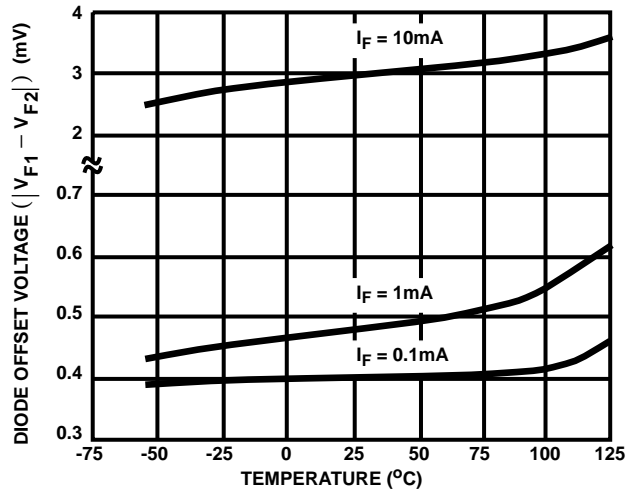


FIGURE 4. DIODE OFFSET VOLTAGE (ANY DIODE) vs TEMPERATURE

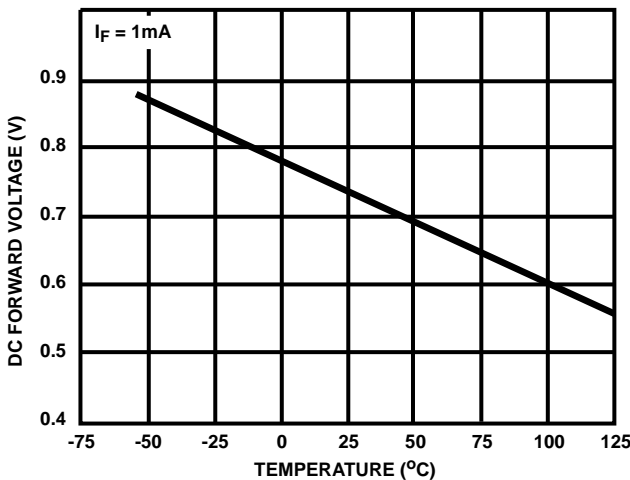


FIGURE 5. DC FORWARD VOLTAGE DROP (ANY DIODE) vs TEMPERATURE

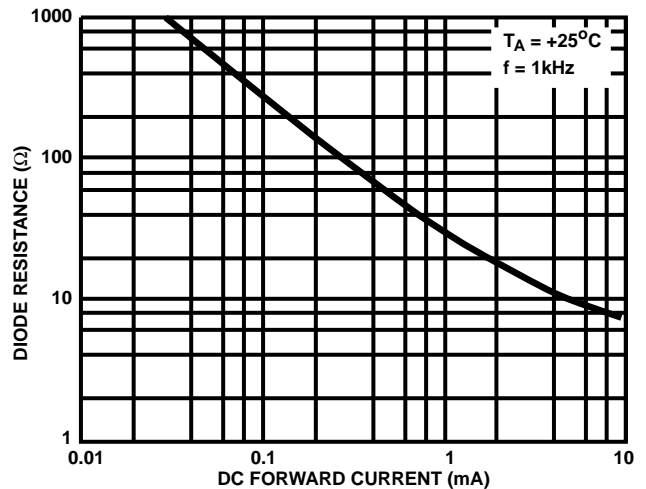


FIGURE 6. DIODE RESISTANCE (ANY DIODE) vs DC FORWARD CURRENT

Typical Performance Curves (Continued)

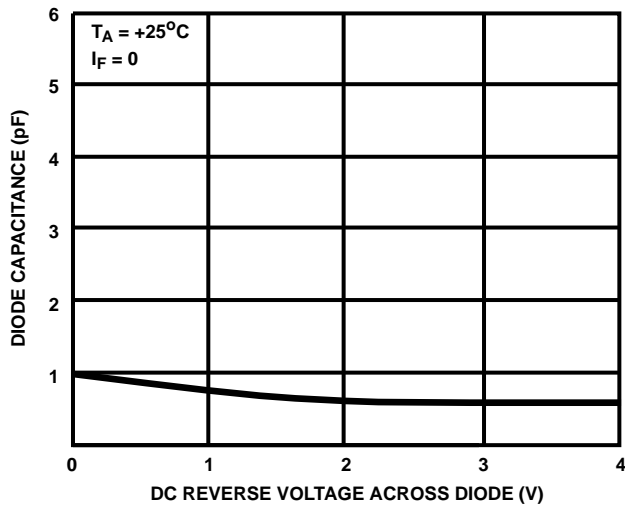


FIGURE 7. DIODE CAPACITANCE ($D_1 - D_5$) vs REVERSE VOLTAGE

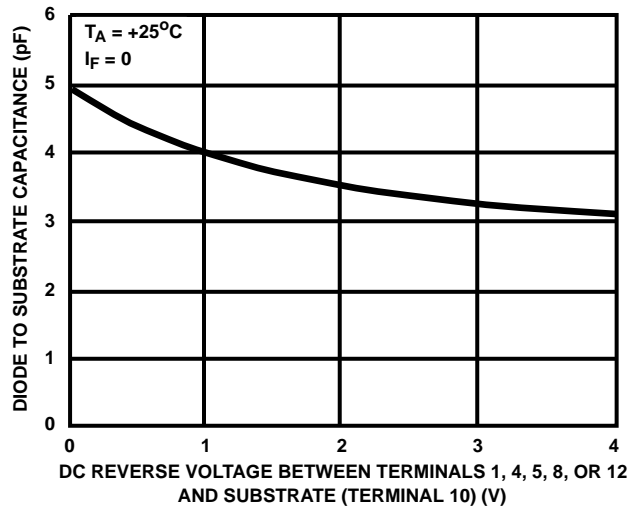


FIGURE 8. DIODE-TO-SUBSTRATE CAPACITANCE vs REVERSE VOLTAGE