



AOP609

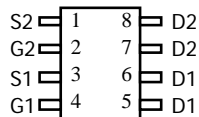
Complementary Enhancement Mode Field Effect Transistor

General Description

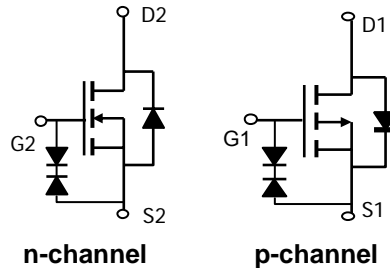
The AOP609 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications. *Standard Product AOP609 is Pb-free (meets ROHS & Sony 259 specifications).*

Features

n-channel	p-channel
V_{DS} (V) = 60V	-60V
$I_D = 4.7A$ ($V_{GS}=10V$)	-3.5A ($V_{GS}=-10V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 60m Ω ($V_{GS}=10V$)	< 115m Ω ($V_{GS}=-10V$)
< 75m Ω ($V_{GS}=4.5V$)	< 140m Ω ($V_{GS}=-4.5V$)
ESD Rating: 1500V HBM	3000V HMB



PDIP-8



n-channel

p-channel

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^A	$T_A=25^\circ\text{C}$	4.7	-3.5	A
	$T_A=70^\circ\text{C}$	3.8	-2.9	
Pulsed Drain Current ^B	I_{DM}	20	-20	
Power Dissipation	$T_A=25^\circ\text{C}$	2.5	2.5	W
	$T_A=70^\circ\text{C}$	1.6	1.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ\text{C}$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	37	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		n-ch	74	90	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	n-ch	28	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	35	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		p-ch	73	90	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	p-ch	32	40	$^\circ\text{C/W}$

N Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=48\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1	μA
					5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			250	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.5	2.4	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=4.7\text{A}$ $T_J=125^\circ\text{C}$		49	60	$\text{m}\Omega$
				65		
		$V_{GS}=4.5\text{V}$, $I_D=3.0\text{A}$		57	75	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=4.7\text{A}$		17		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.78	1	V
I_S	Maximum Body-Diode Continuous Current				3.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=30\text{V}$, $f=1\text{MHz}$		450	570	pF
C_{oss}	Output Capacitance			74		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		1.65	2	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$, $I_D=4.7\text{A}$		5.1	7	nC
$Q_g(4.5\text{V})$	Total Gate Charge			2.5	3	nC
Q_{gs}	Gate Source Charge			1		nC
Q_{gd}	Gate Drain Charge			1.4		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$, $R_L=6\Omega$, $R_{GEN}=3\Omega$		5.4		ns
t_r	Turn-On Rise Time			5.5		ns
$t_{D(off)}$	Turn-Off DelayTime			17.2		ns
t_f	Turn-Off Fall Time			2.9		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=4.7\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		25.4	35	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=4.7\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		29.4		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

Rev 2 : Sept 2007

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

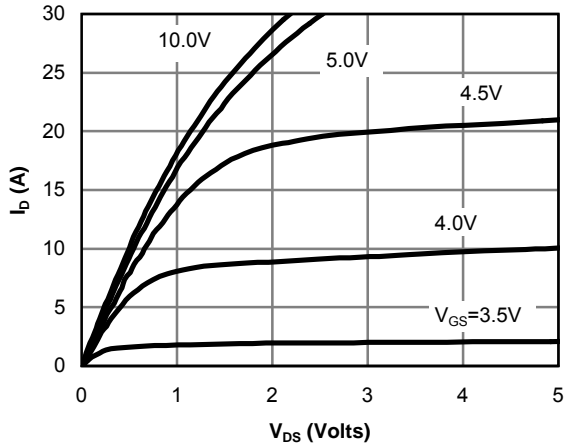


Fig 1: On-Region Characteristics

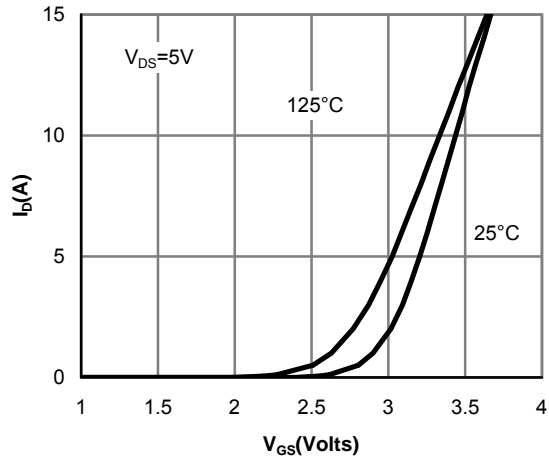


Figure 2: Transfer Characteristics

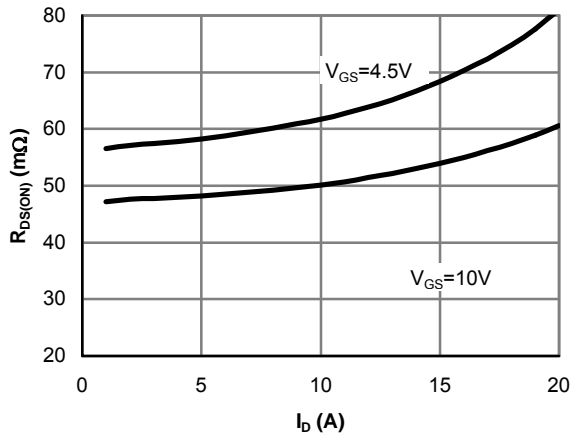


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

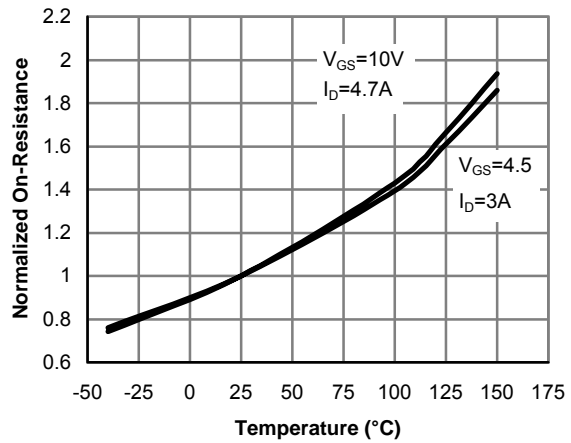


Figure 4: On-Resistance vs. Junction Temperature

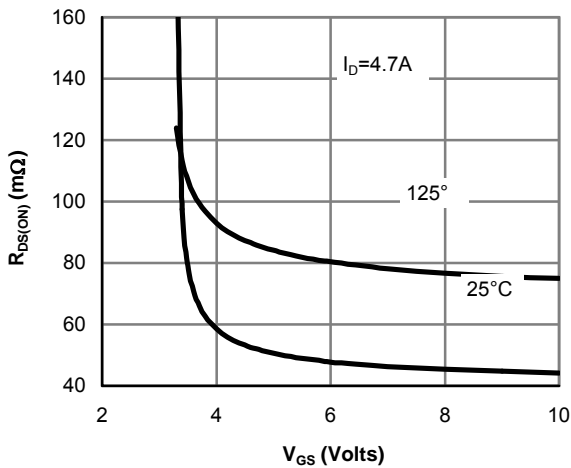


Figure 5: On-Resistance vs. Gate-Source Voltage

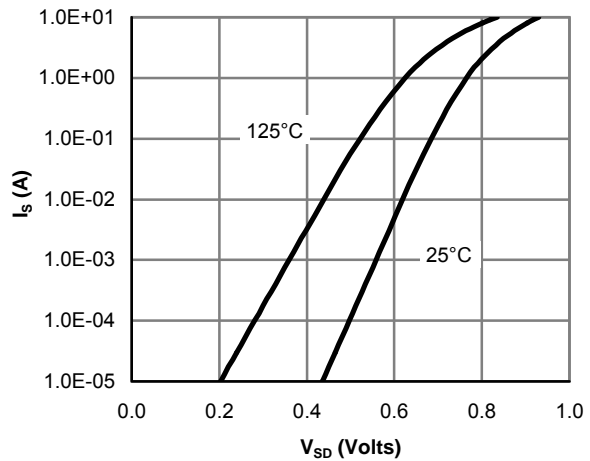


Figure 6: Body-Diode Characteristics

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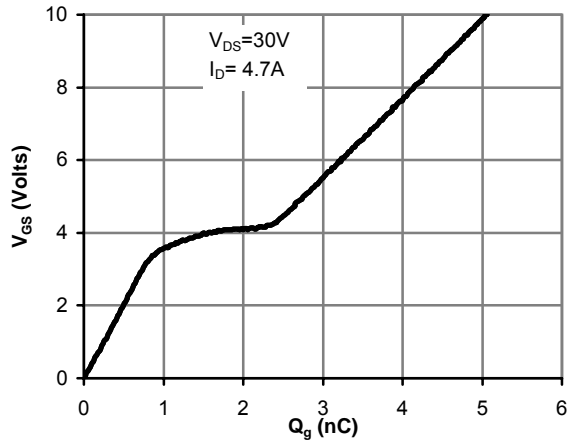


Figure 7: Gate-Charge Characteristics

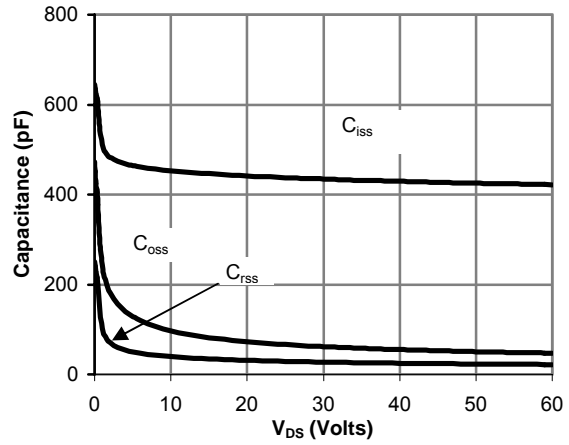


Figure 8: Capacitance Characteristics

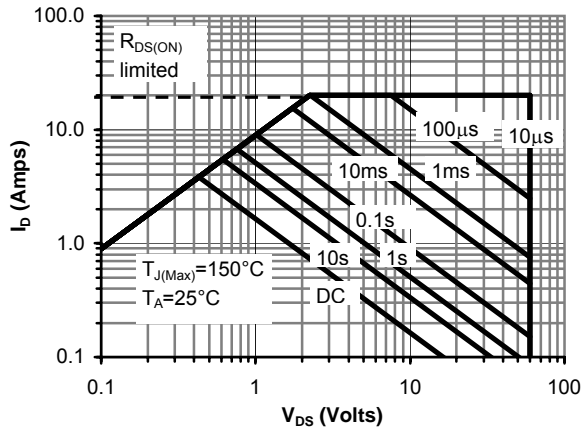


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

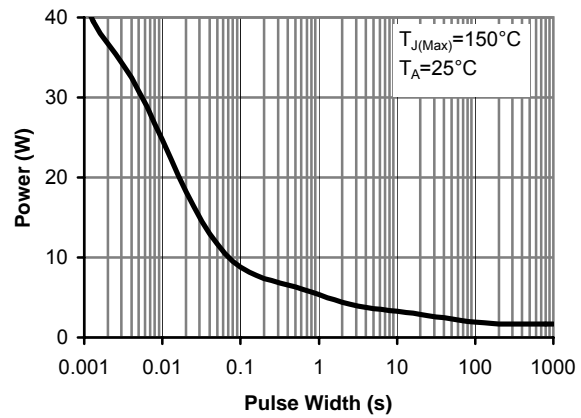


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

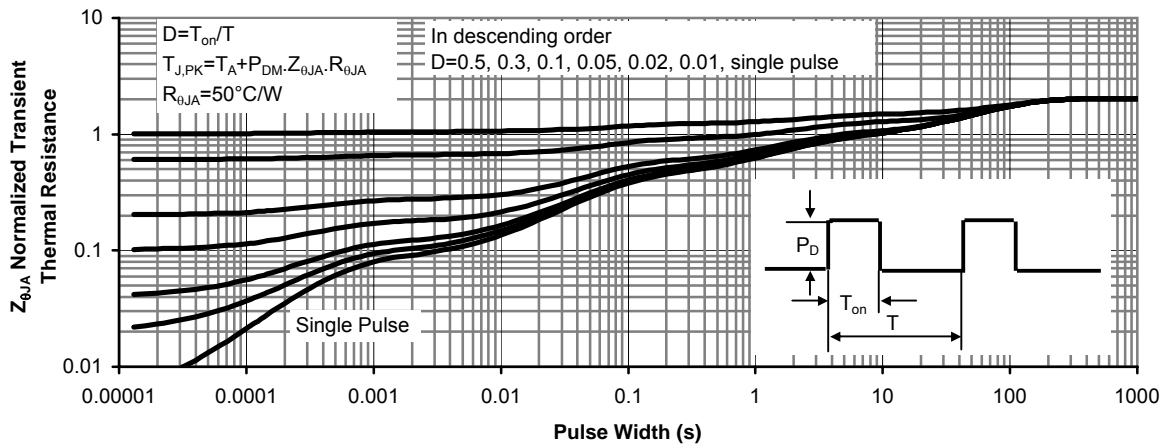


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}, V_{GS}=0\text{V}$	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-48\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			100	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1.5	-1.8	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}, V_{DS}=-5\text{V}$	-20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}, I_D=-3.5\text{A}$ $T_J=125^\circ\text{C}$		95 133	115	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}, I_D=-2.8\text{A}$		112	140	
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}, I_D=-3.5\text{A}$		9		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}, V_{GS}=0\text{V}$		-0.77	-1	V
I_S	Maximum Body-Diode Continuous Current				-3.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=-30\text{V}, f=1\text{MHz}$		897	1080	pF
C_{oss}	Output Capacitance			88		pF
C_{rss}	Reverse Transfer Capacitance			36		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		7.2	9	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}, V_{DS}=-30\text{V}, I_D=-3.5\text{A}$		8.1	10	nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			3.9	5	nC
Q_{gs}	Gate Source Charge			1.4		nC
Q_{gd}	Gate Drain Charge			1.7		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=-10\text{V}, V_{DS}=-30\text{V}, R_L=8.1\Omega,$ $R_{GEN}=3\Omega$		9		ns
t_r	Turn-On Rise Time			7.2		ns
$t_{D(off)}$	Turn-Off Delay Time			35		ns
t_f	Turn-Off Fall Time			25.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-3.5\text{A}, dI/dt=100\text{A}/\mu\text{s}$		25.8	35	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-3.5\text{A}, dI/dt=100\text{A}/\mu\text{s}$		28.8		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

Rev2:Sept 2007

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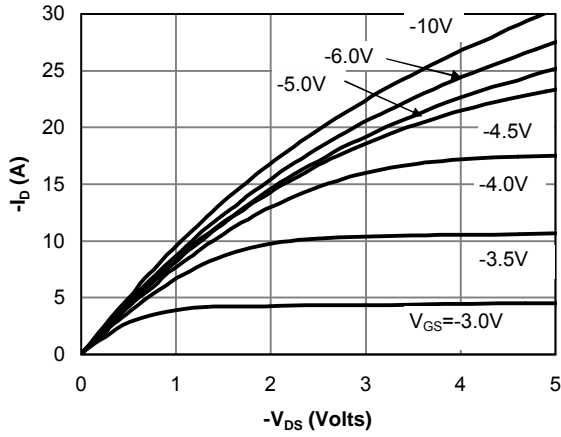


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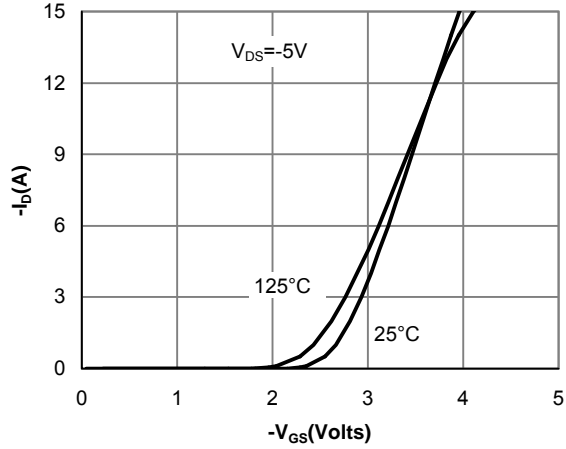


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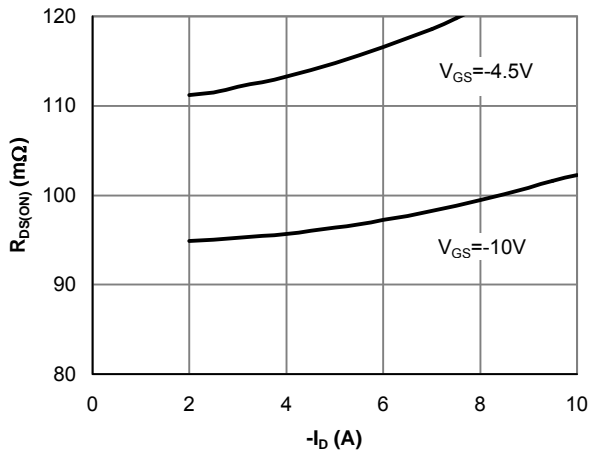


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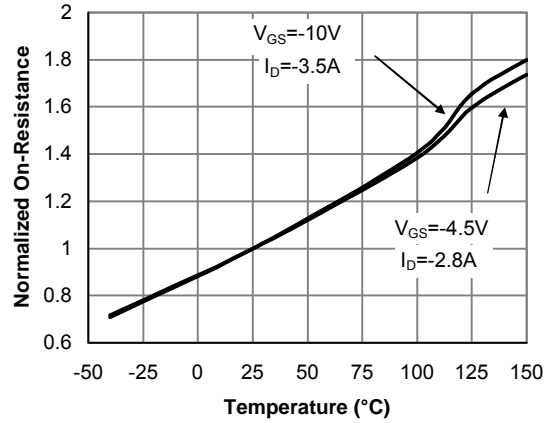


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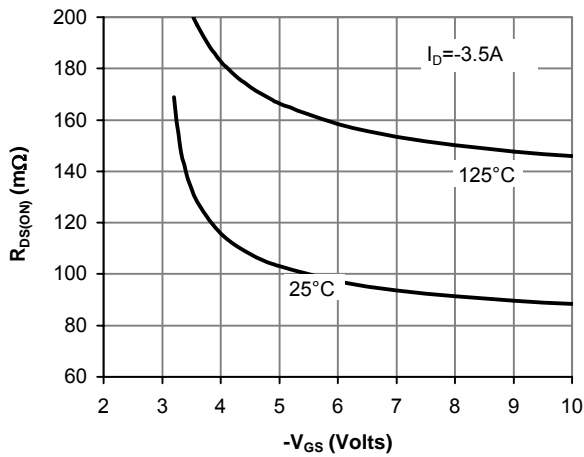


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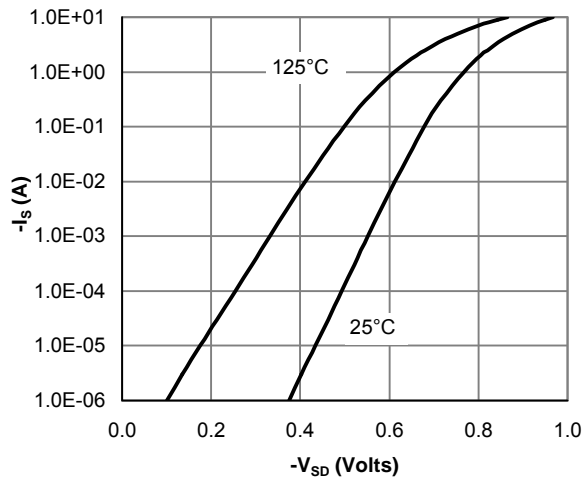


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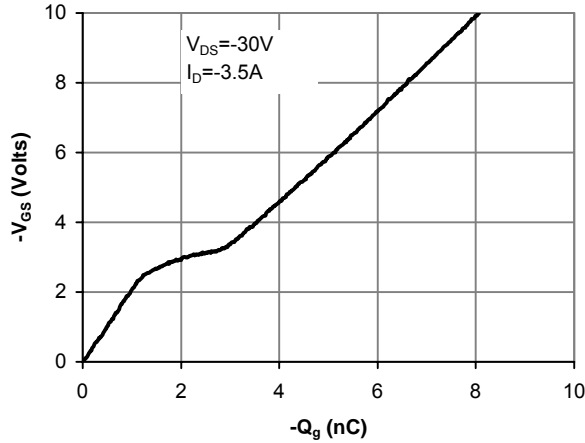


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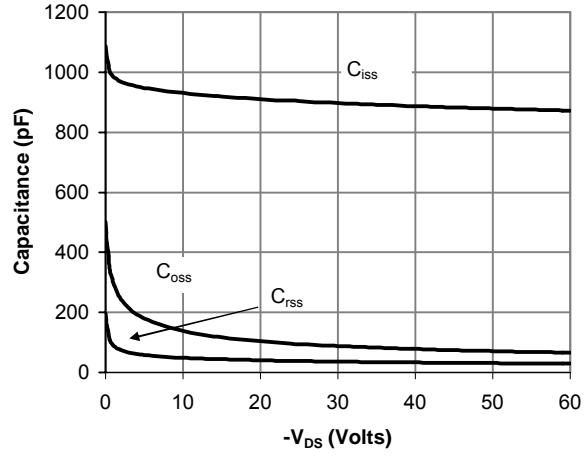


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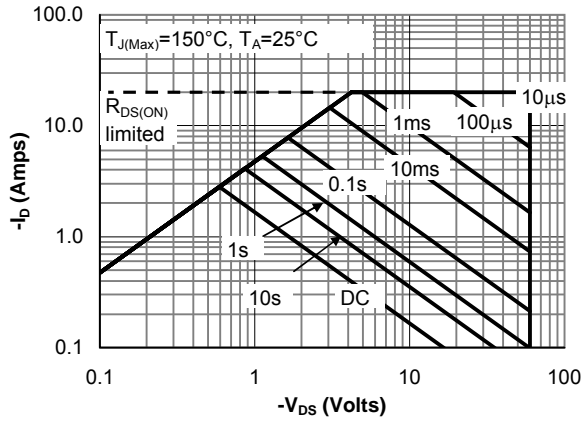


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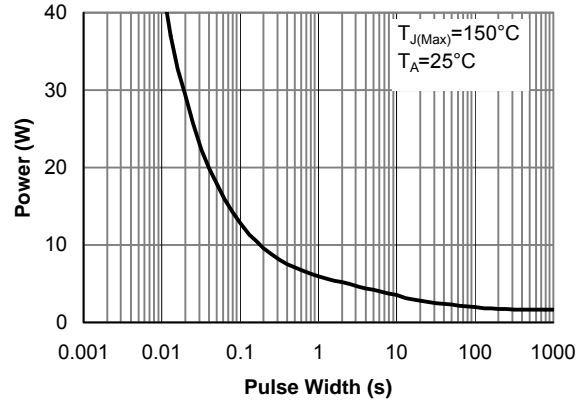


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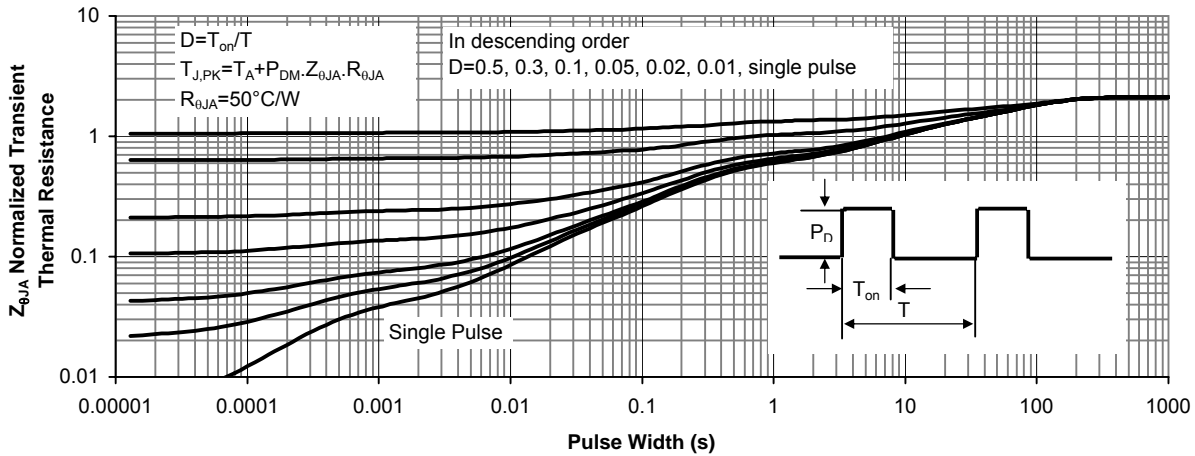


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