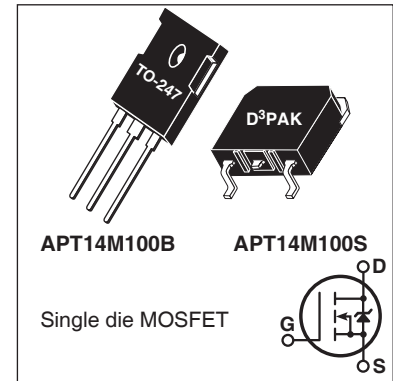



N-Channel MOSFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. A proprietary planar stripe design yields excellent reliability and manufacturability. Low switching loss is achieved with low input capacitance and ultra low C_{rss} "Miller" capacitance. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control slew rates during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency. Reliability in flyback, boost, forward, and other circuits is enhanced by the high avalanche energy capability.



FEATURES

- Fast switching with low EMI/RFI
- Low $R_{DS(on)}$
- Ultra low C_{rss} for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant 

TYPICAL APPLICATIONS

- PFC and other boost converter
- Buck converter
- Two switch forward (asymmetrical bridge)
- Single switch forward
- Flyback
- Inverters

Absolute Maximum Ratings

| Symbol | Parameter | Ratings | Unit |
|----------|--|---------|------|
| I_D | Continuous Drain Current @ $T_C = 25^\circ\text{C}$ | 14 | A |
| | Continuous Drain Current @ $T_C = 100^\circ\text{C}$ | 9 | |
| I_{DM} | Pulsed Drain Current ^① | 56 | |
| V_{GS} | Gate-Source Voltage | ±30 | V |
| E_{AS} | Single Pulse Avalanche Energy ^② | 875 | mJ |
| I_{AR} | Avalanche Current, Repetitive or Non-Repetitive | 7 | A |

Thermal and Mechanical Characteristics

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-----------------|--|-----|------|------|--------|
| P_D | Total Power Dissipation @ $T_C = 25^\circ\text{C}$ | | | 500 | W |
| $R_{\theta JC}$ | Junction to Case Thermal Resistance | | | 0.25 | °C/W |
| $R_{\theta CS}$ | Case to Sink Thermal Resistance, Flat, Greased Surface | | 0.11 | | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 | | 150 | °C |
| T_L | Soldering Temperature for 10 Seconds (1.6mm from case) | | | 300 | |
| W_T | Package Weight | | 0.22 | | oz |
| | | | 6.2 | | g |
| Torque | Mounting Torque (TO-264 Package), 4-40 or M3 screw | | | 10 | in-lbf |
| | | | | 1.1 | N-m |

Static Characteristics
T_J = 25°C unless otherwise specified
APT14M100B_S

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------------------------------|---|--|------|------|------|-------|
| V _{BR(DSS)} | Drain-Source Breakdown Voltage | V _{GS} = 0V, I _D = 250μA | 1000 | | | V |
| ΔV _{BR(DSS)/ΔT_J} | Breakdown Voltage Temperature Coefficient | Reference to 25°C, I _D = 250μA | | 1.15 | | V/°C |
| R _{DS(on)} | Drain-Source On Resistance ^③ | V _{GS} = 10V, I _D = 7A | | 0.73 | 0.90 | Ω |
| V _{GS(th)} | Gate-Source Threshold Voltage | V _{GS} = V _{DS} , I _D = 1mA | 3 | 4 | 5 | V |
| ΔV _{GS(th)/ΔT_J} | Threshold Voltage Temperature Coefficient | | | -10 | | mV/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 1000V V _{GS} = 0V | | | 100 | μA |
| | | T _J = 25°C T _J = 125°C | | | 500 | |
| I _{GSS} | Gate-Source Leakage Current | V _{GS} = ±30V | | | ±100 | nA |

Dynamic Characteristics
T_J = 25°C unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------|--|---|-----|------|-----|------|
| g _{fs} | Forward Transconductance | V _{DS} = 50V, I _D = 7A | | 16 | | S |
| C _{iss} | Input Capacitance | V _{GS} = 0V, V _{DS} = 25V f = 1MHz | | 3965 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 55 | | |
| C _{oss} | Output Capacitance | | | 335 | | |
| C _{o(cr)} ^④ | Effective Output Capacitance, Charge Related | V _{GS} = 0V, V _{DS} = 0V to 667V | | 135 | | pF |
| C _{o(er)} ^⑤ | Effective Output Capacitance, Energy Related | | | 70 | | |
| Q _g | Total Gate Charge | V _{GS} = 0 to 10V, I _D = 7A, V _{DS} = 500V | | 120 | | nC |
| Q _{gs} | Gate-Source Charge | | | 21 | | |
| Q _{gd} | Gate-Drain Charge | | | 60 | | |
| t _{d(on)} | Turn-On Delay Time | Resistive Switching V _{DD} = 667V, I _D = 7A R _G = 4.7Ω ^⑥ , V _{GG} = 15V | | 18 | | ns |
| t _r | Current Rise Time | | | 16 | | |
| t _{d(off)} | Turn-Off Delay Time | | | 60 | | |
| t _f | Current Fall Time | | | 15 | | |

Source-Drain Diode Characteristics

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-----------------|---|--|-----|------|-----|------|
| I _S | Continuous Source Current (Body Diode) | MOSFET symbol showing the integral reverse p-n junction diode (body diode) | | | 14 | A |
| I _{SM} | Pulsed Source Current (Body Diode) ^① | | | | 56 | |
| V _{SD} | Diode Forward Voltage | I _{SD} = 7A, T _J = 25°C, V _{GS} = 0V | | | 1 | V |
| t _{rr} | Reverse Recovery Time | I _{SD} = 7A, V _{DD} = 100V ^② di _{SD} /dt = 100A/μs, T _J = 25°C | | 1065 | | ns |
| Q _{rr} | Reverse Recovery Charge | | | 22 | | μC |
| dv/dt | Peak Recovery dv/dt | I _{SD} ≤ 7A, di/dt ≤ 1000A/μs, V _{DD} = 667V, T _J = 125°C | | | 10 | V/ns |

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at T_J = 25°C, L = 35.71mH, R_G = 4.7Ω, I_{AS} = 7A.

③ Pulse test: Pulse Width < 380μs, duty cycle < 2%.

④ C_{o(cr)} is defined as a fixed capacitance with the same stored charge as C_{OSS} with V_{DS} = 67% of V_{(BR)DSS}.

⑤ C_{o(er)} is defined as a fixed capacitance with the same stored energy as C_{OSS} with V_{DS} = 67% of V_{(BR)DSS}. To calculate C_{o(er)} for any value of V_{DS} less than V_{(BR)DSS}, use this equation: C_{o(er)} = -1.15E-7/V_{DS}² + 2.03E-8/V_{DS} + 3.93E-11.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

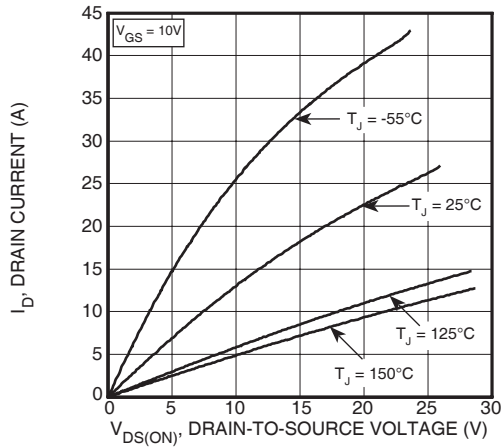


Figure 1, Output Characteristics

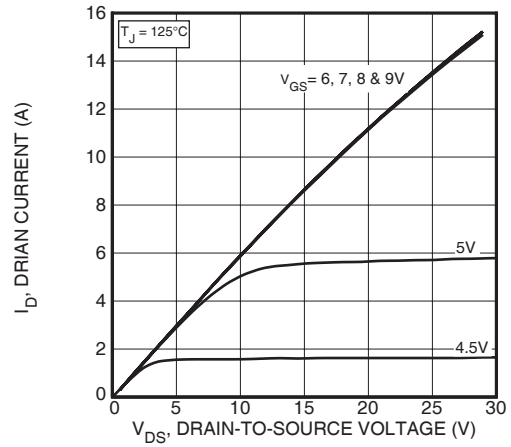


Figure 2, Output Characteristics

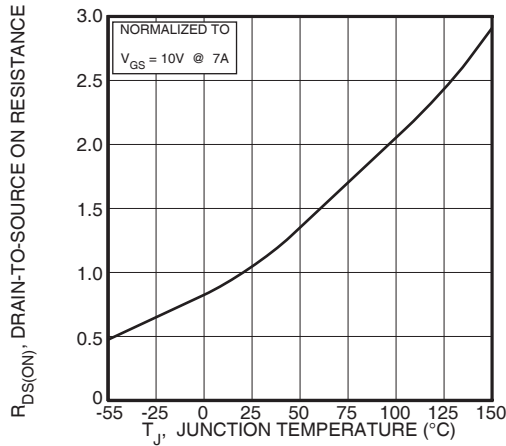


Figure 3, $R_{DS(ON)}$ vs Junction Temperature

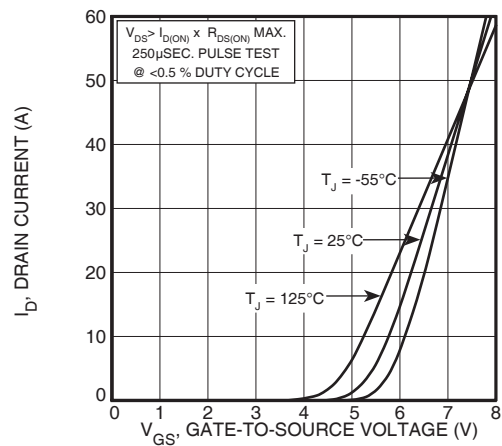


Figure 4, Transfer Characteristics

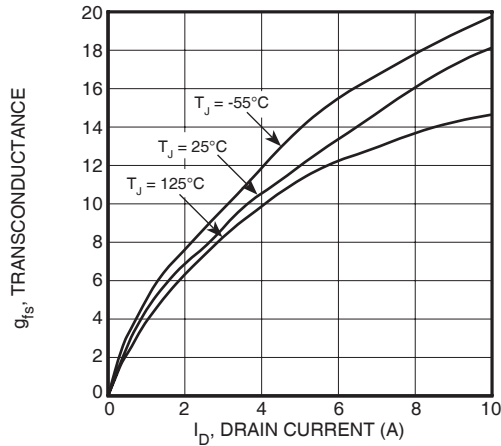


Figure 5, Gain vs Drain Current

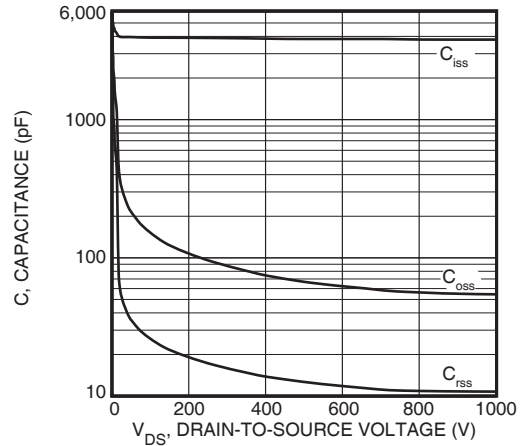


Figure 6, Capacitance vs Drain-to-Source Voltage

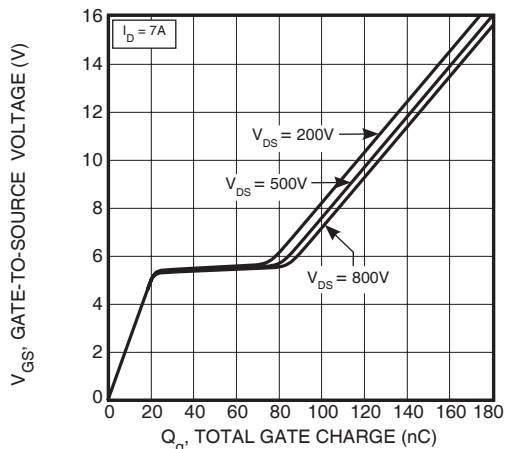


Figure 7, Gate Charge vs Gate-to-Source Voltage

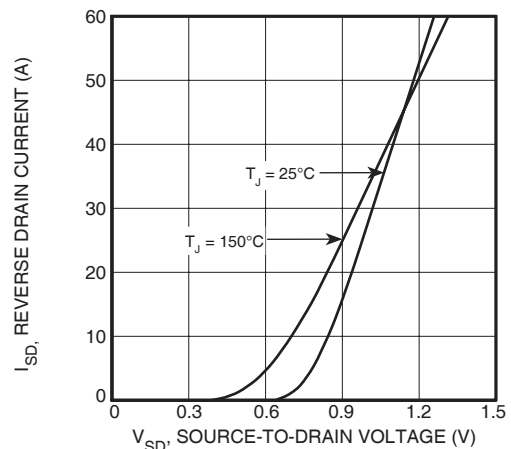


Figure 8, Reverse Drain Current vs Source-to-Drain Voltage

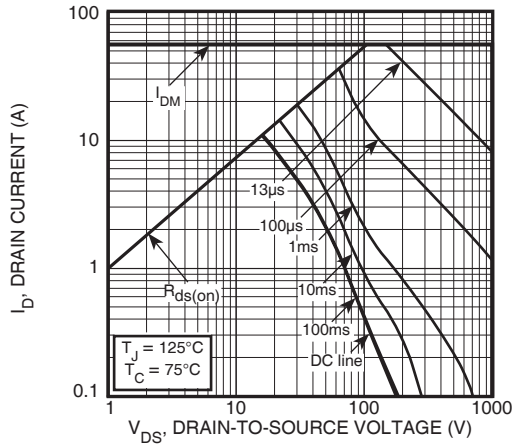


Figure 9, Forward Safe Operating Area

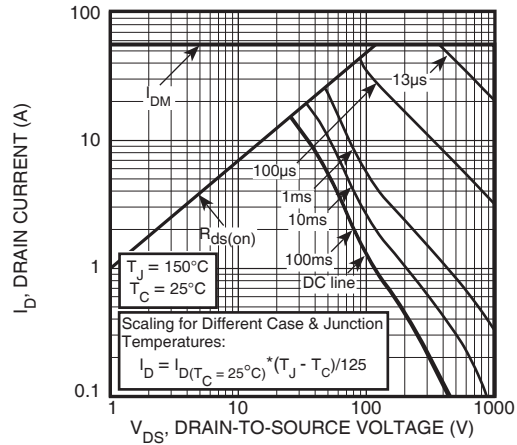


Figure 10, Maximum Forward Safe Operating Area

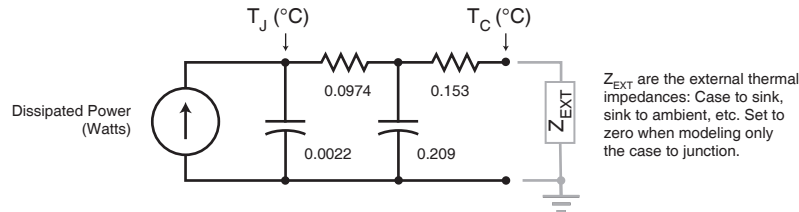


Figure 11, Transient Thermal Impedance Model

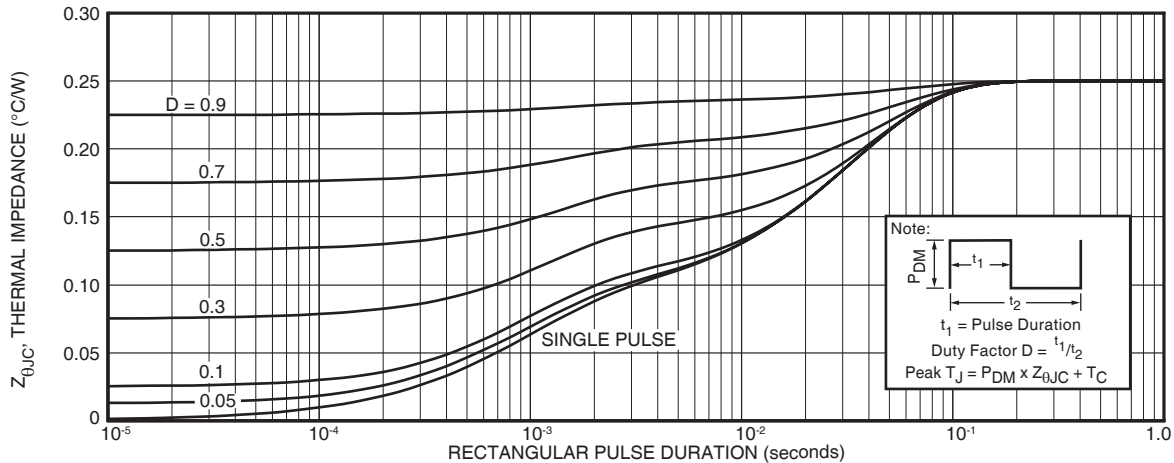
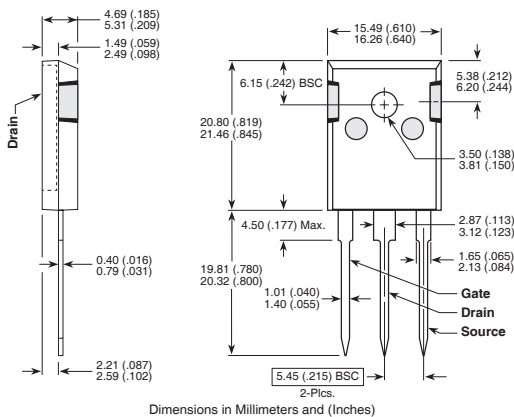
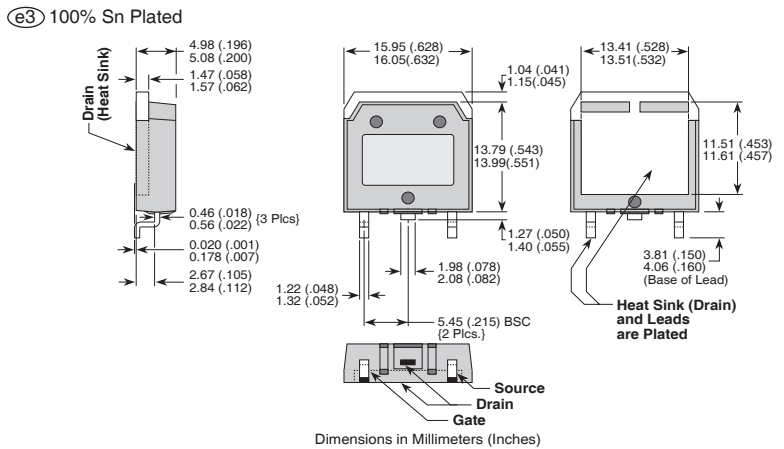


Figure 12. Maximum Effective Transient Thermal Impedance Junction-to-Case vs. Pulse Duration

TO-247 (B) Package Outline



D³PAK Package Outline



050-8105 Rev A 2-2007