AON3814
Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

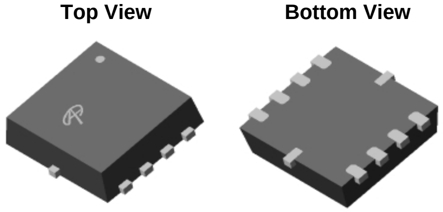
The AON3814 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V while retaining a 12V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration. *Standard Product AON3814 is Pb-free (meets ROHS & Sony 259 specifications).*

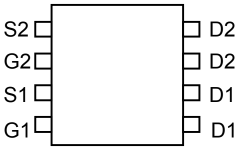
Features

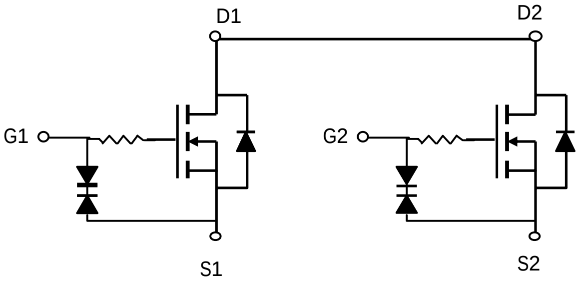
V_{DS} (V) = 20V
I_D = 6A (V_{GS} = 4.5V)
$R_{DS(ON)} < 17m\Omega$ (V_{GS} = 4.5V)
$R_{DS(ON)} < 18.5m\Omega$ (V_{GS} = 4V)
$R_{DS(ON)} < 24m\Omega$ (V_{GS} = 2.5V)
$R_{DS(ON)} < 39m\Omega$ (V_{GS} = 1.8V)

ESD Protected

DFN 3x3







Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current ^{F}	T_A=25°C	I_D	6	A
	T_A=70°C		5.3	
Pulsed Drain Current ^{B}		I_{DM}	30	
Power Dissipation ^{F}	T_A=25°C	P_D	2.4	W
	T_A=70°C		1.5	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient ^{A}	t ≤ 10s	$R_{\theta JA}$	43	52	°C/W
Maximum Junction-to-Ambient ^{A}	Steady-State		75	90	°C/W
Maximum Junction-to-Lead ^{C}	Steady-State	$R_{\theta JL}$	36	50	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±10V			10	µA
BV_{GSO}	Gate-Source Breakdown Voltage	V_{DS}=0V, I_G=±250µA	±12			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	0.4	0.71	1.1	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=6A		14	17	mΩ
		T_J=125°C		19	24	
		V_{GS}=4V, I_D=6A		15	18.5	mΩ
		V_{GS}=2.5V, I_D=6A		19	24	
		V_{GS}=1.8V, I_D=6A		30	39	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=6A		25		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				3.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=10V, f=1MHz		1315		pF
C_{oss}	Output Capacitance			219		pF
C_{rss}	Reverse Transfer Capacitance			183		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2.1		kΩ
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=10V, I_D=6A		13.1		nC
Q_{gs}	Gate Source Charge			6.7		nC
Q_{gd}	Gate Drain Charge			4.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=5V, V_{DS}=10V, R_L=1.7Ω, R_{GEN}=3Ω		1		µs
t_r	Turn-On Rise Time			2.8		µs
$t_{D(off)}$	Turn-Off DelayTime			5.6		µs
t_f	Turn-Off Fall Time			5.9		µs

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
F. The power dissipation and current rating is based on the t ≤ 10s thermal resistance, and current rating is also limited by wire-bonding.
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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

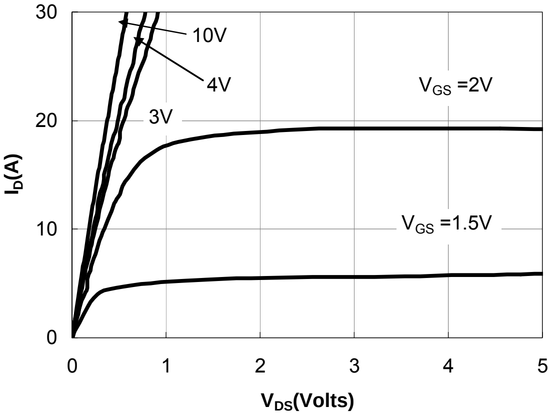

Figure 1: On-Regions Characteristics

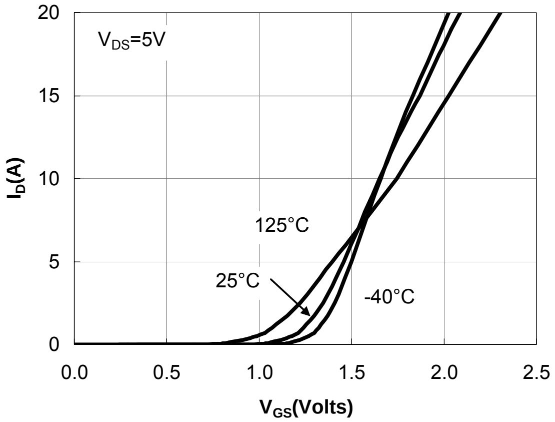

Figure 2: Transfer Characteristics

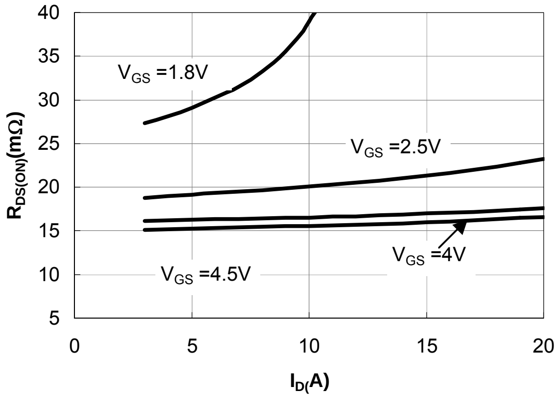

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

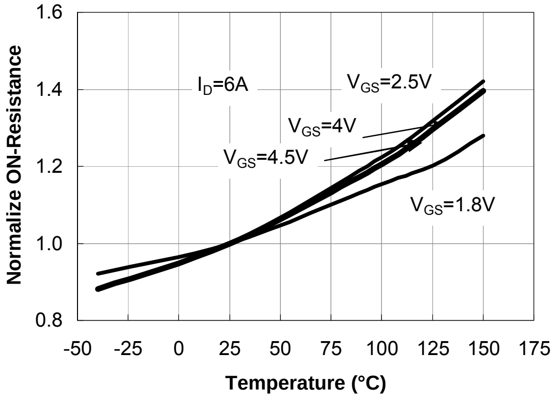

Figure 4: On-Resistance vs. Junction Temperature

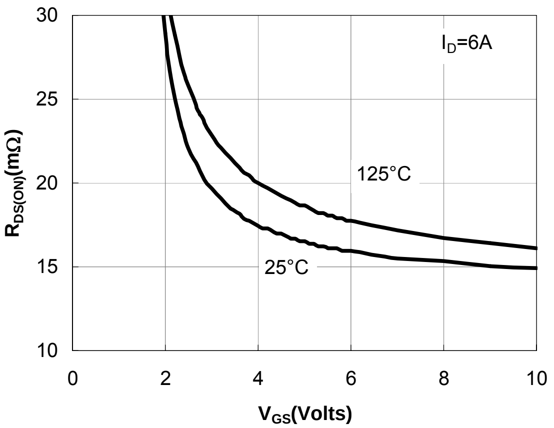

Figure 5: On-Resistance vs. Gate-Source Voltage

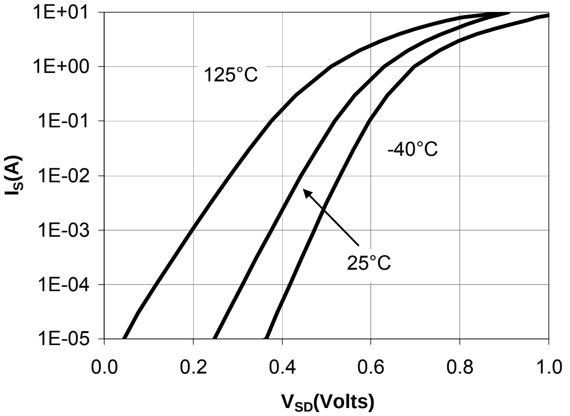

Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

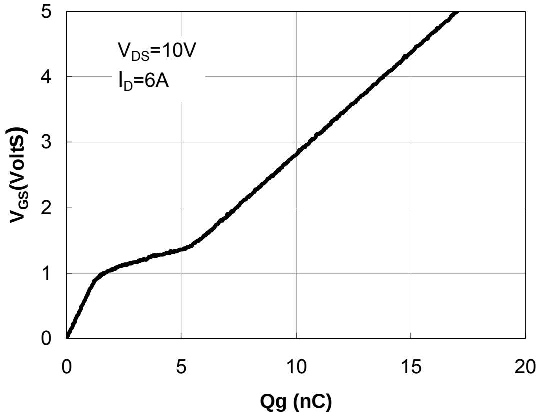

Figure 7: Gate-Charge Characteristics

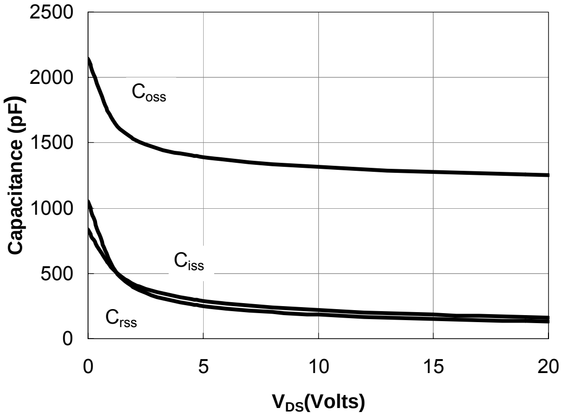

Figure 8: Capacitance Characteristics

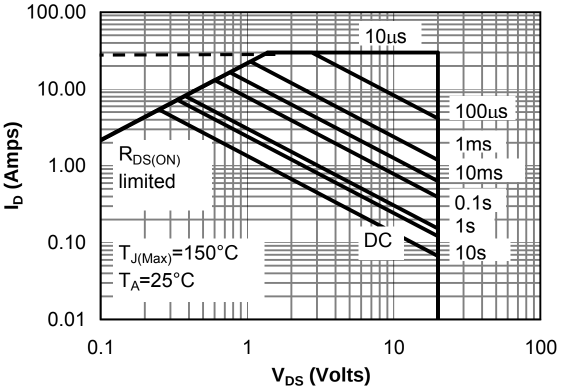

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

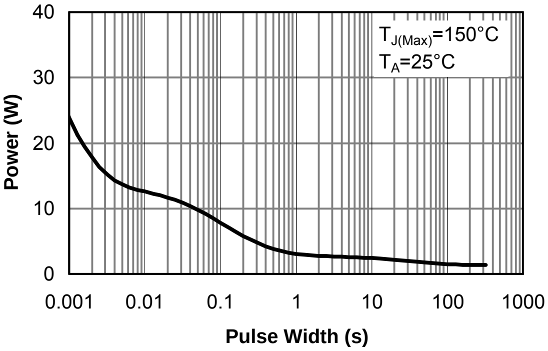

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

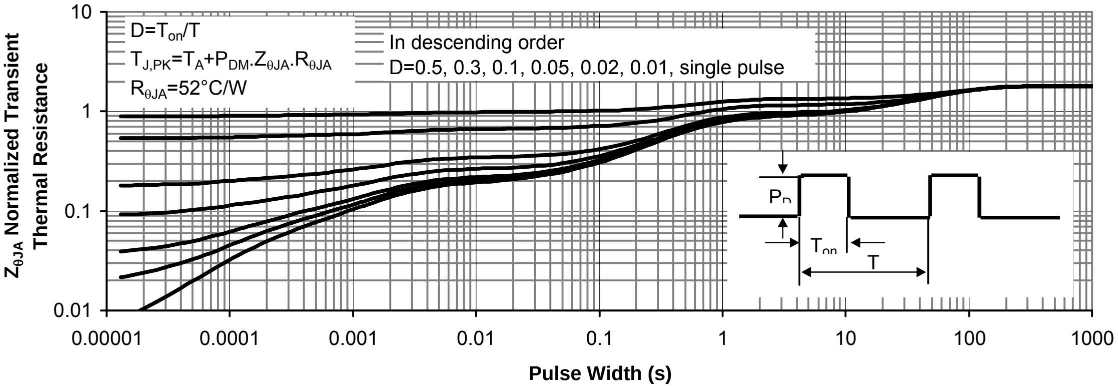

Figure 11: Normalized Maximum Transient Thermal Impedance