

Plastic Medium-Power Complementary Silicon Transistors

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
 $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ Adc
- Collector Emitter Sustaining Voltage — @ 100 mAdc
 $V_{CE(sus)} = 80$ Vdc (Min) — BDX53B, 54B
 $= 100$ Vdc (Min) — BDX53C, 54C
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 3.0$ Adc
 $= 4.0$ Vdc (Max) @ $I_C = 5.0$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package

MAXIMUM RATINGS

Rating	Symbol	BDX53B BDX54B	BDX53C BDX54C	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	8.0 12		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	60 0.48		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	70	$^\circ\text{C/W}$

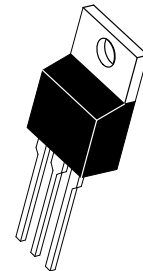
NPN
BDX53B

BDX53C

PNP
BDX54B

BDX54C

DARLINGTON
8 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80-100 VOLTS
65 WATTS



CASE 221A-06
TO-220AB

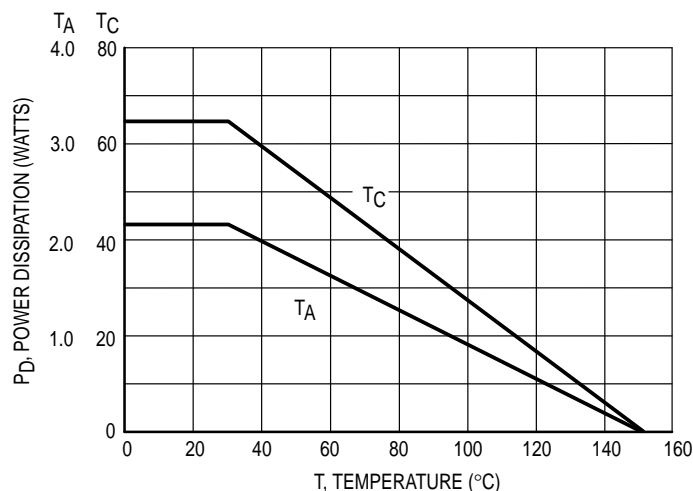


Figure 1. Power Derating

BDX53B BDX53C BDX54B BDX54C

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) ($I_C = 100\text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector Cutoff Current ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$)	I_{CEO}	— —	0.5 0.5	mAdc
Collector Cutoff Current ($V_{CB} = 80\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100\text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	0.2 0.2	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$)	h_{FE}	750	—	—
Collector–Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 12\text{ mAdc}$)	$V_{CE(sat)}$	— —	2.0 4.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_C = 12\text{ mA}$)	$V_{BE(sat)}$	—	2.5	Vdc

DYNAMIC CHARACTERISTICS

Small–Signal Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	h_{fe}	4.0	—	—
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	— —	300 200	pF

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

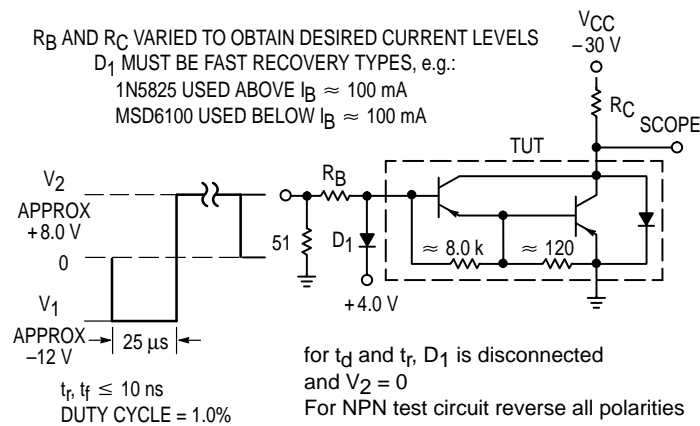


Figure 2. Switching Time Test Circuit

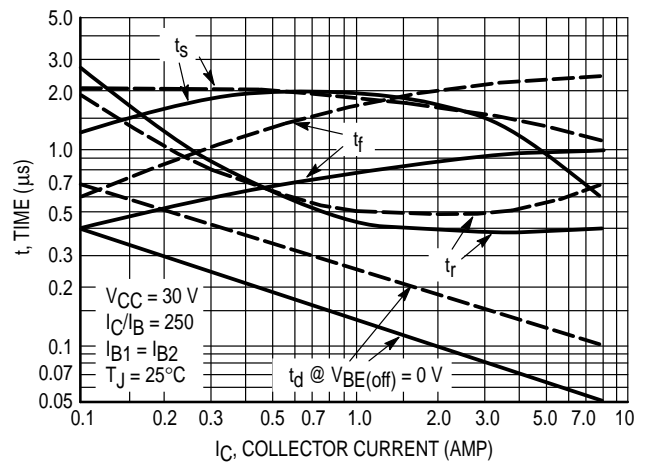


Figure 3. Switching Times

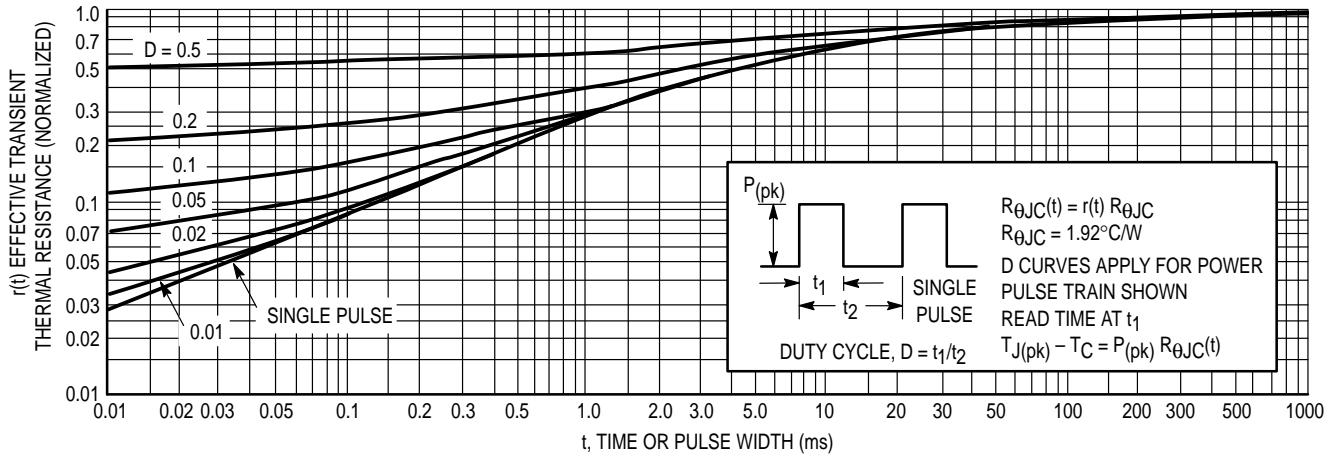


Figure 4. Thermal Response

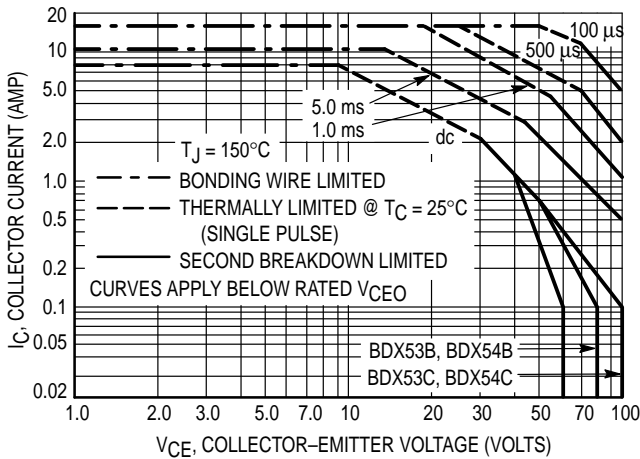


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

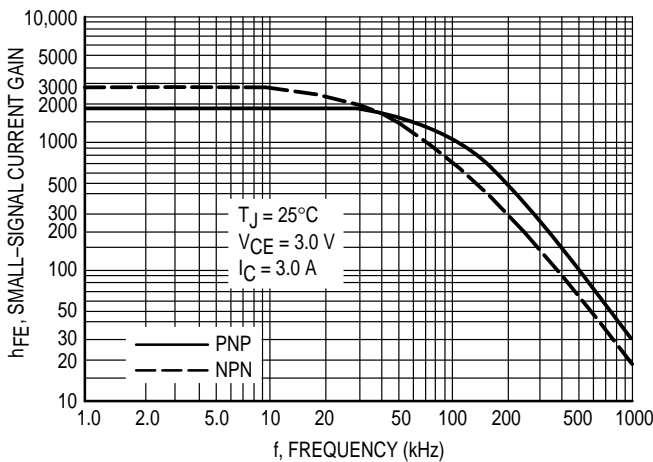


Figure 6. Small-Signal Current Gain

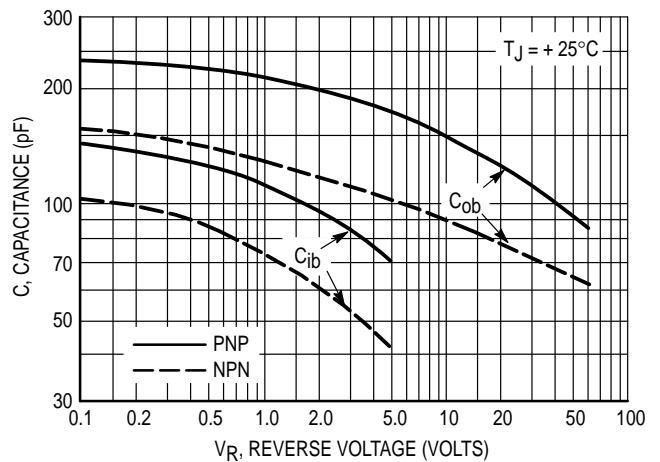
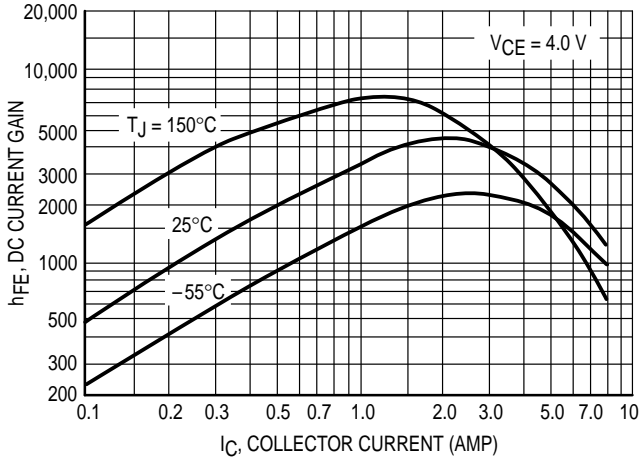


Figure 7. Capacitance

BDX53B BDX53C BDX54B BDX54C

**NPN
BDX53B, 53C**



**PNP
BDX54B, 54C**

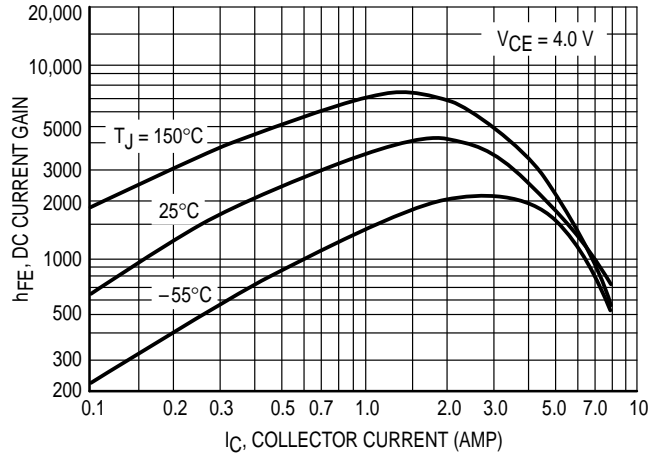


Figure 8. DC Current Gain

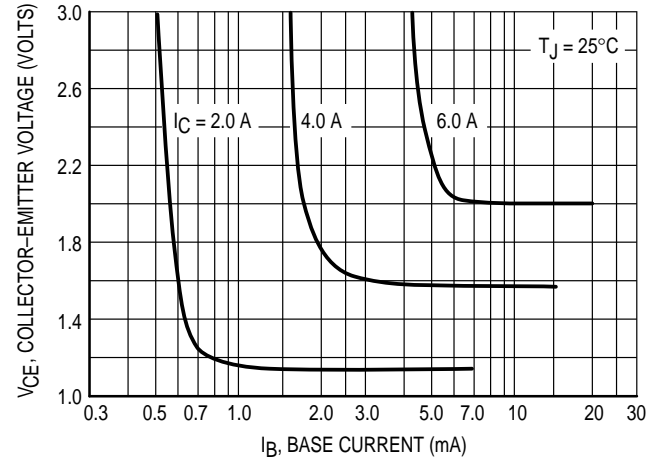
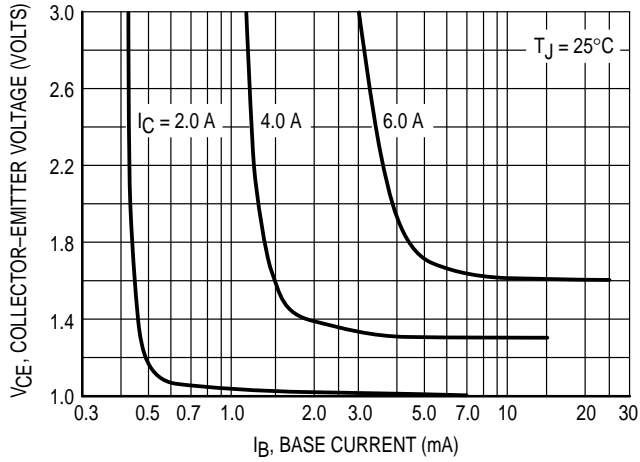


Figure 9. Collector Saturation Region

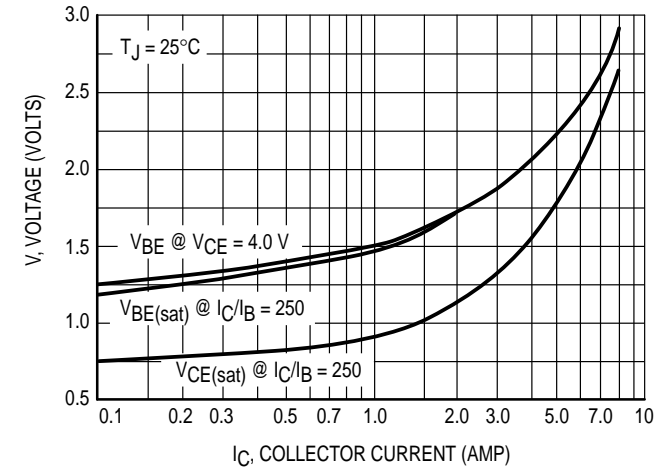
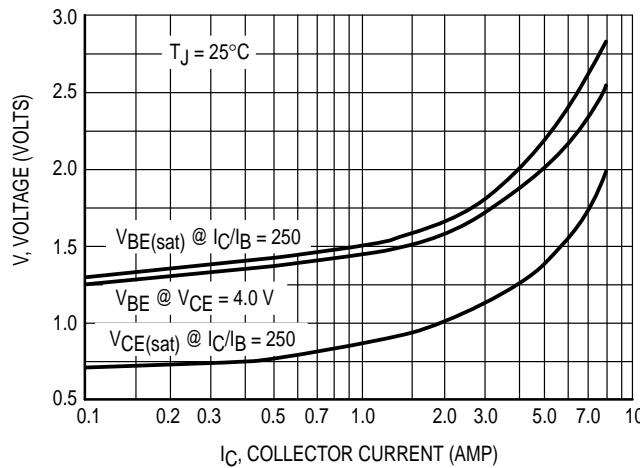


Figure 10. "On" Voltages

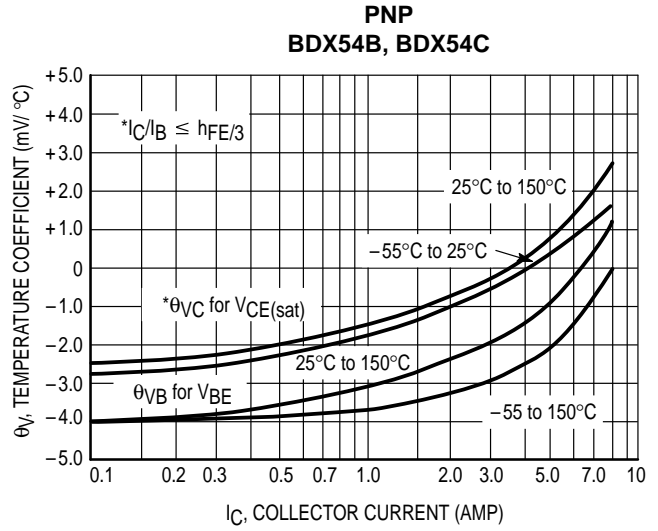
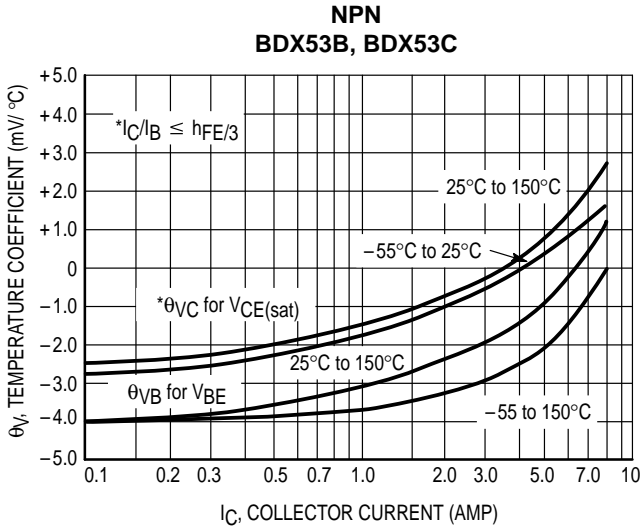


Figure 11. Temperature Coefficients

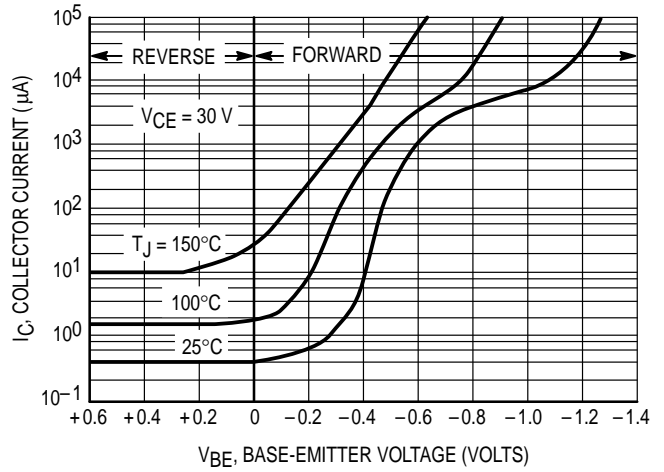
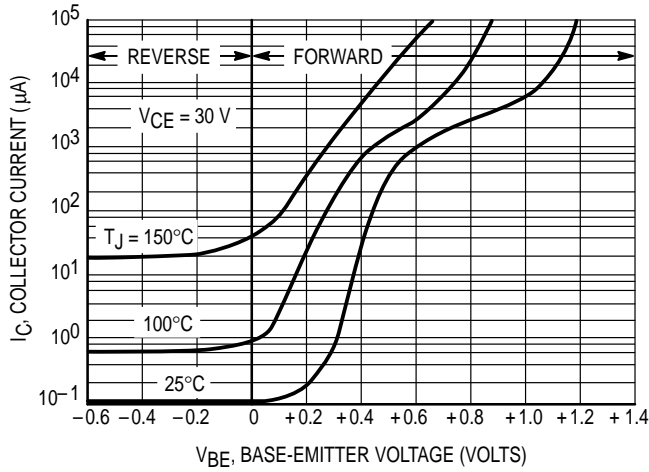


Figure 12. Collector Cut-Off Region

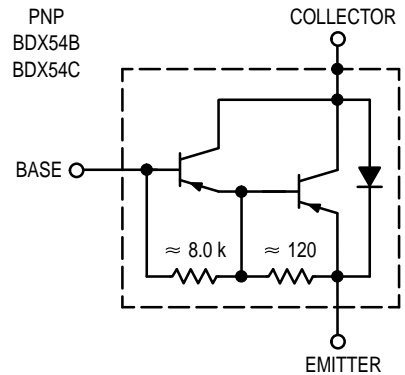
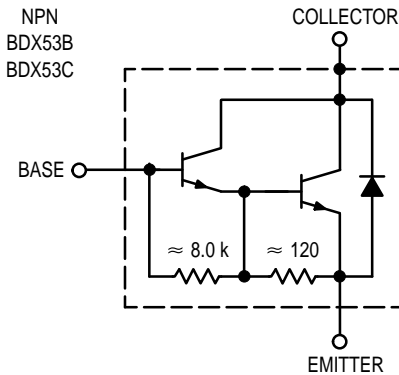
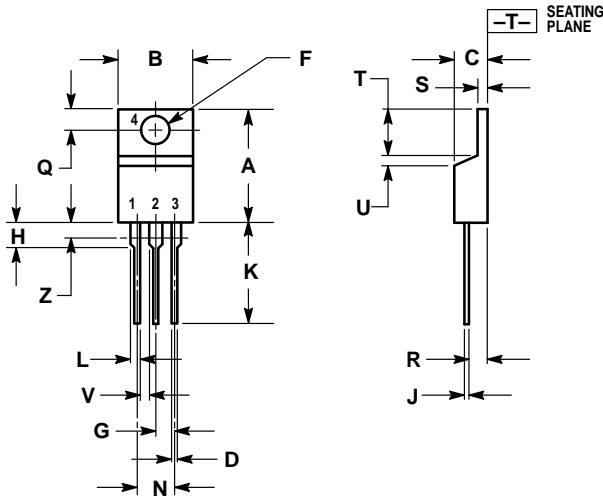


Figure 13. Darlington Schematic

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

- STYLE 1:
1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

**CASE 221A-06
TO-220AB
ISSUE Y**

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