

**AOL1436**  
**N-Channel Enhancement Mode Field Effect Transistor**
**General Description**

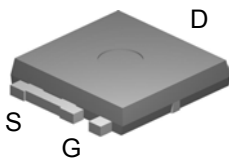
The AOL1436 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , shoot-through immunity and body diode characteristics. This device is ideally suited for use as a High side switch in CPU core power conversion. *Standard Product AOL1436 is Pb-free (meets ROHS & Sony 259 specifications).*

**Features**

$V_{DS} (V) = 25V$   
 $I_D = 50A (V_{GS} = 10V)$   
 $R_{DS(ON)} < 6m\Omega (V_{GS} = 20V)$   
 $R_{DS(ON)} < 8.2m\Omega (V_{GS} = 12V)$   
 $R_{DS(ON)} < 11.5m\Omega (V_{GS} = 10V)$

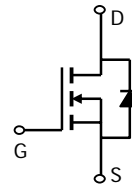
**UIS Tested!**  
**Rg,Ciss,Coss,Crss Tested!**

Ultra SO-8™ Top View



Bottom tab  
connected to  
drain

**Fits SOIC8  
footprint !**


**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Continuous Drain Current <sup>B</sup>	$T_C=25^\circ C^G$	50	A
		$T_C=100^\circ C$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	120	
Continuous Drain Current <sup>A</sup>	$T_A=25^\circ C$	20	A
	$T_A=70^\circ C$	$I_{DSM}$ 16	
Avalanche Current <sup>C</sup>	$I_{AR}$	28	A
Repetitive avalanche energy $L=0.3mH^C$	$E_{AR}$	118	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ C$	$P_D$ 43	W
	$T_C=100^\circ C$	22	
Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	$P_{DSM}$ 5	W
	$T_A=70^\circ C$	3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

**Thermal Characteristics**

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$t \leq 10s$	$R_{\theta JA}$	20	25	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A</sup>	Steady-State		46	55	$^\circ C/W$
Maximum Junction-to-Case <sup>D</sup>	Steady-State	$R_{\theta JC}$	2.5	3.5	$^\circ C/W$

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	25			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 30\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2	3.2	4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=12\text{V}$ , $V_{DS}=5\text{V}$	120			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=20\text{V}$ , $I_D=20\text{A}$		5	6	$\text{m}\Omega$
		$V_{GS}=12\text{V}$ , $I_D=20\text{A}$		6.6	8.2	$\text{m}\Omega$
		$V_{GS}=10\text{V}$ , $I_D=20\text{A}$ $T_J=125^\circ\text{C}$		8.6 11	11.5	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=20\text{A}$		43		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.72	1	V
$I_S$	Maximum Body-Diode Continuous Current				50	A
<b>DYNAMIC PARAMETERS</b>						
$C_{ISS}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=12.5\text{V}$ , $f=1\text{MHz}$		1100	1350	pF
$C_{OSS}$	Output Capacitance		420		pF	
$C_{RSS}$	Reverse Transfer Capacitance		200		pF	
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		0.8	1.5	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(12\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=12.5\text{V}$ , $I_D=20\text{A}$		20	24	nC
$Q_g(10\text{V})$	Total Gate Charge		17			
$Q_{gs}$	Gate Source Charge		6.5		nC	
$Q_{gd}$	Gate Drain Charge		6.8		nC	
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$ , $V_{DS}=12.5\text{V}$ , $R_L=0.68\Omega$ , $R_{GEN}=0.6\Omega$		9.5		ns
$t_r$	Turn-On Rise Time		13.5		ns	
$t_{D(off)}$	Turn-Off Delay Time		11.5		ns	
$t_f$	Turn-Off Fall Time		5.4		ns	
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=20\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		32		ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		19		nC

A. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $t < 10\text{s}$   $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $< 300\mu\text{s}$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^\circ\text{C}$ . The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ .

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

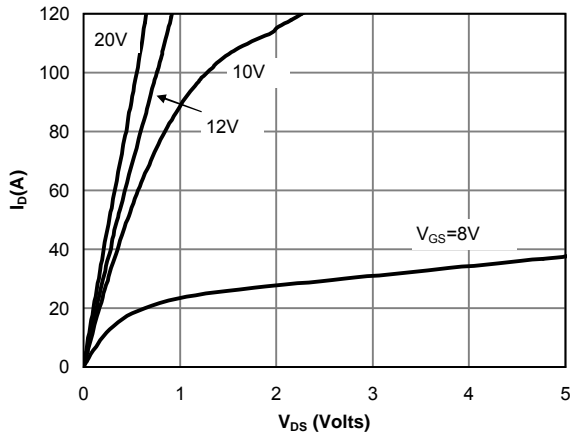


Figure 1: On-Region Characteristics

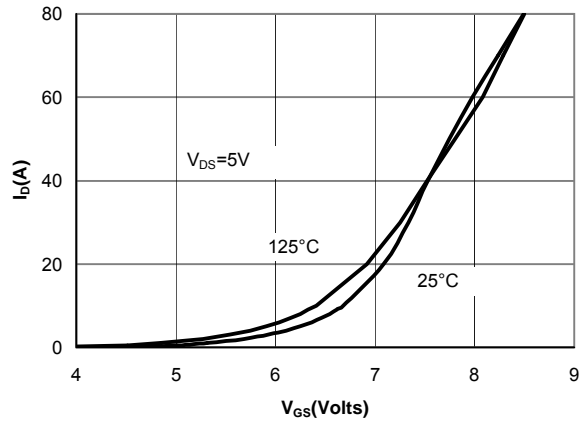


Figure 2: Transfer Characteristics

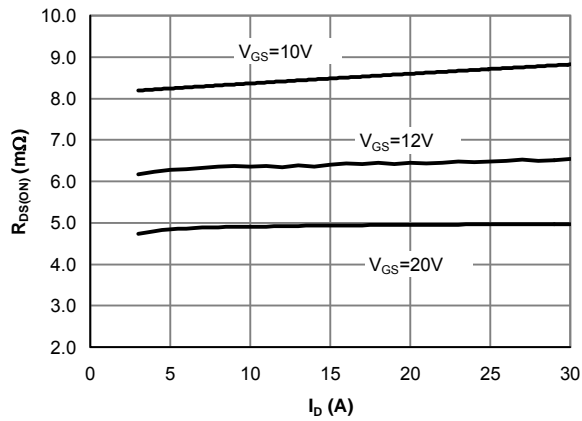


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

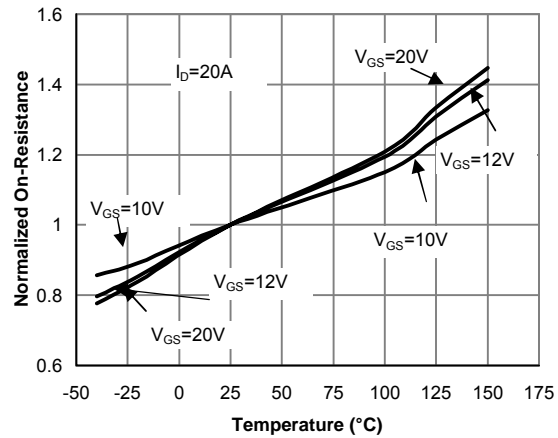


Figure 4: On-Resistance vs. Junction Temperature

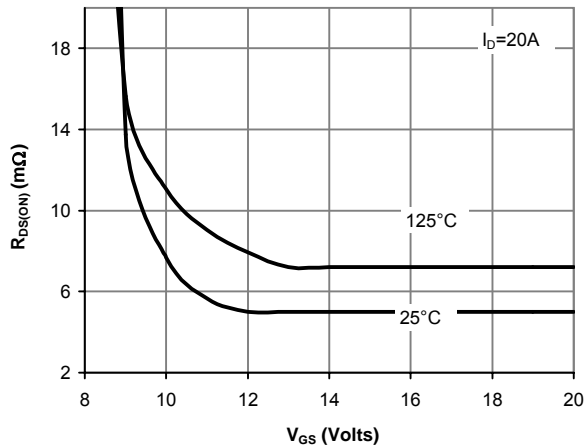


Figure 5: On-Resistance vs. Gate-Source Voltage

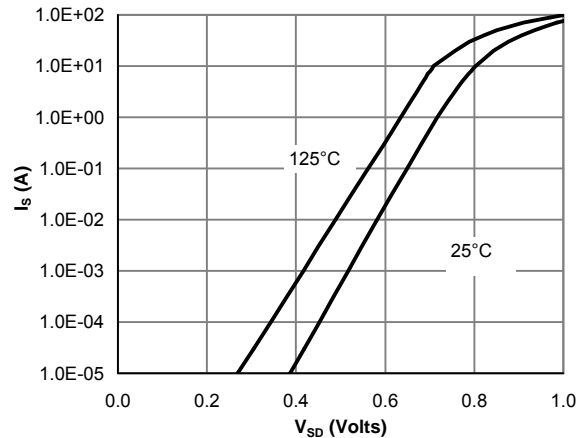


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

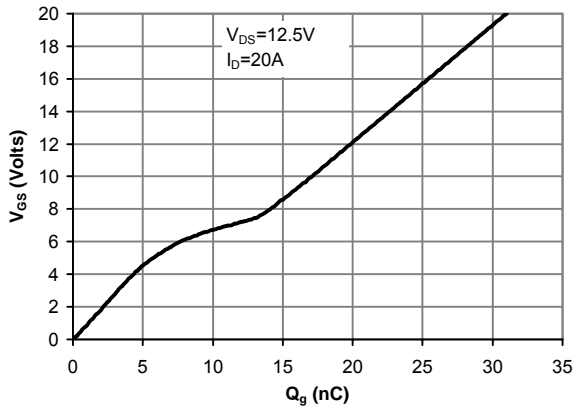


Figure 7: Gate-Charge Characteristics

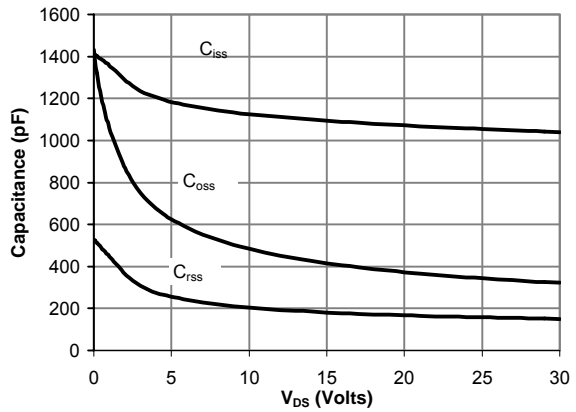


Figure 8: Capacitance Characteristics

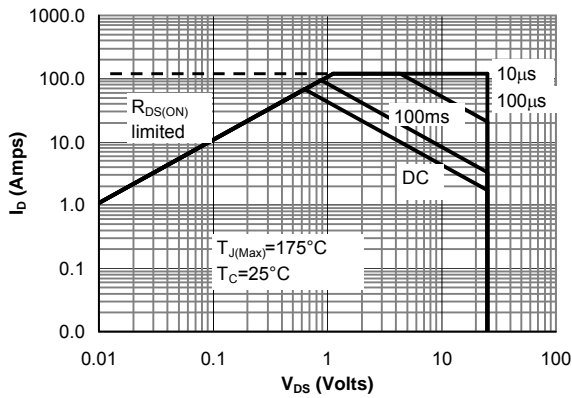


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

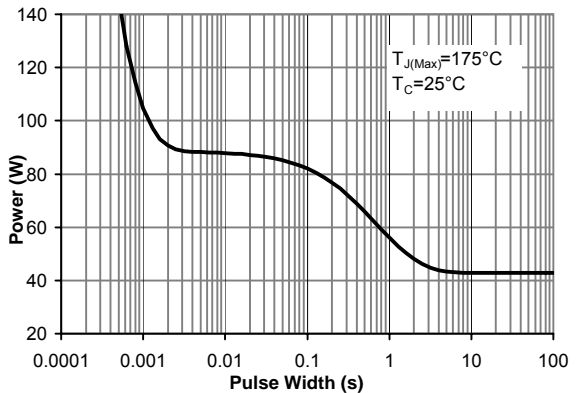


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

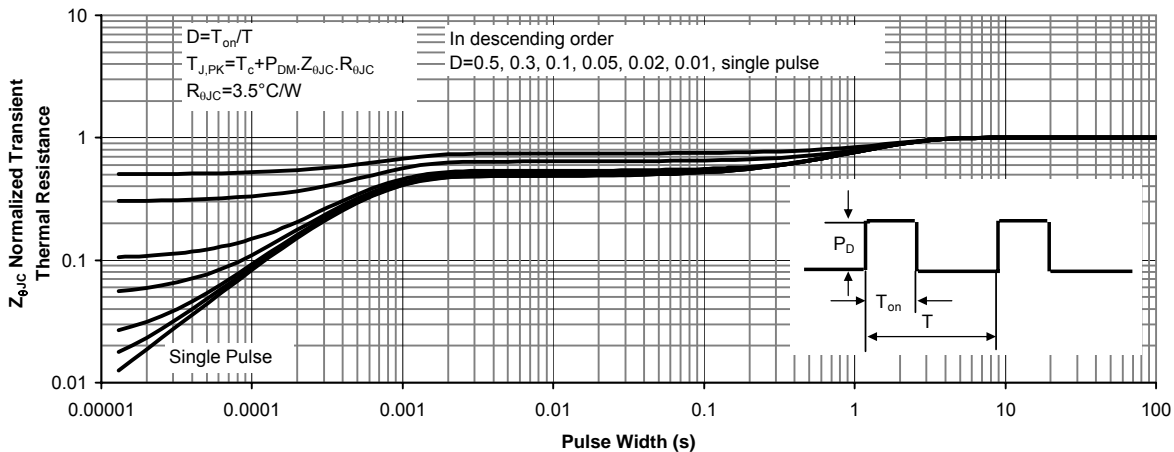


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

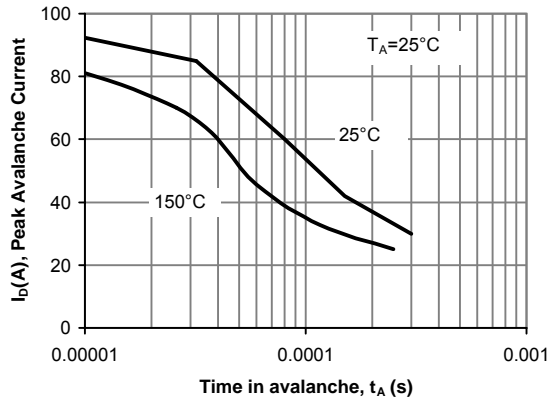


Figure 12: Single Pulse Avalanche capability

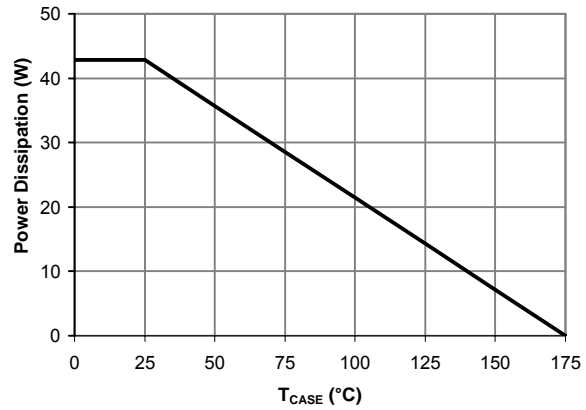


Figure 13: Power De-rating (Note B)

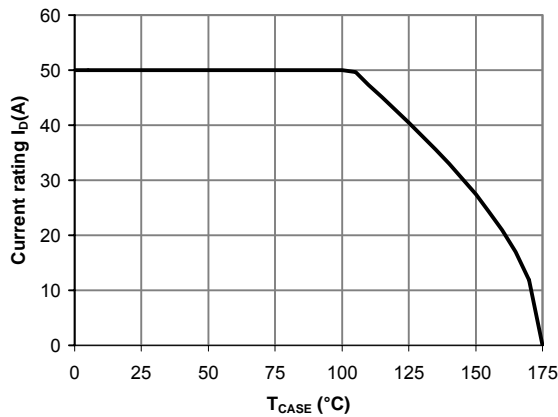


Figure 14: Current De-rating (Note B)

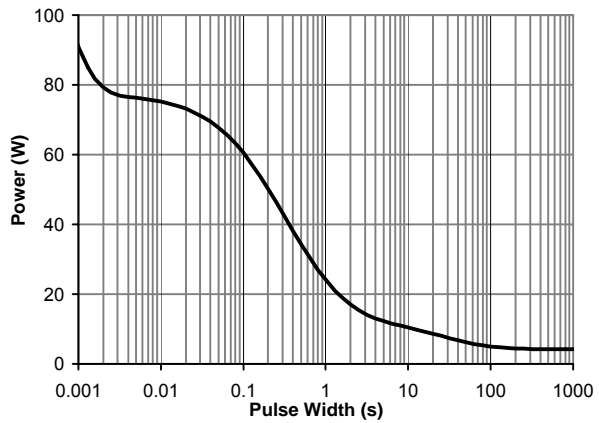


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

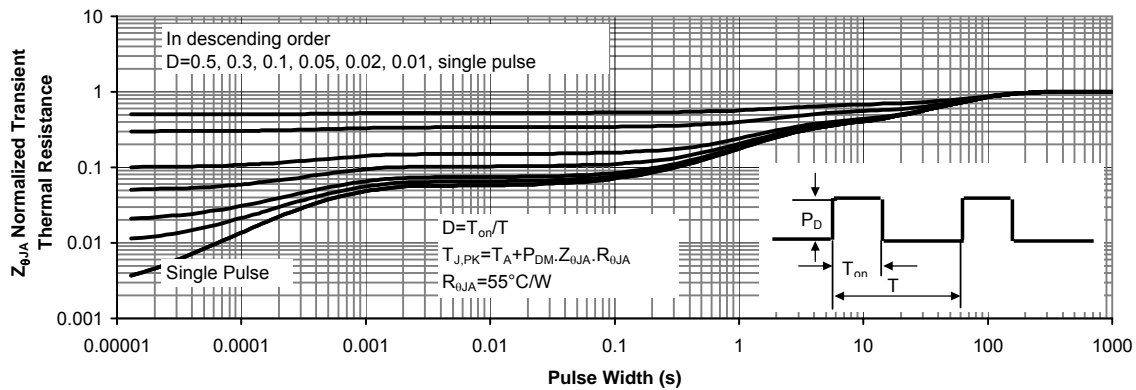


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)