

**AOL1413**  
**P-Channel Enhancement Mode Field Effect Transistor**

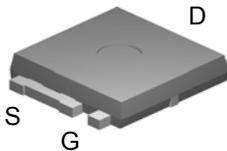
**General Description**

The AOL1413 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and ultra-low low gate charge with a 25V gate rating. This device is suitable for use as a load switch or in PWM applications. The device is ESD protected. *Standard product AOL1413 is Pb-free (meets ROHS & Sony 259 specifications).*

**Features**

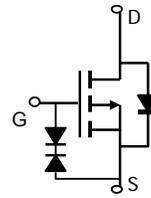
$V_{DS}$  (V) = -30V  
 $I_D$  = -20A ( $V_{GS}$  = -10V)  
 $R_{DS(ON)}$  < 17m $\Omega$  ( $V_{GS}$  = -10V)  
 $R_{DS(ON)}$  < 36m $\Omega$  ( $V_{GS}$  = -5V)  
 ESD Protected!

Ultra SO-8™ Top View



Bottom tab  
connected to  
drain

**Fits SOIC8  
footprint !**


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current <sup>B</sup>	$I_D$	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-70	A
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	18	$^\circ\text{C/W}$
		Steady-State	49	
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	2.9	4	$^\circ\text{C/W}$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±25V			±10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.5	-2.5	-3.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-70			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A T <sub>J</sub> =125°C		13.5 18.5	17 24	mΩ
		V <sub>GS</sub> =-5V, I <sub>D</sub> =-20A		28	36	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =20A		27		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		-0.72	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-40	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz		1760	2200	pF
C <sub>OSS</sub>	Output Capacitance			360		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			255		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		6.4	8	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-20A		30	38	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			11		nC
Q <sub>gs</sub>	Gate Source Charge			7		nC
Q <sub>gd</sub>	Gate Drain Charge			8		nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		11.5		ns
t <sub>r</sub>	Turn-On Rise Time			8		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			35		ns
t <sub>f</sub>	Turn-Off Fall Time			18.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-20A, dI/dt=100A/μs		24	30	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-20A, dI/dt=100A/μs		16		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on t<10s R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 us pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

Rev0: Sep, 2007

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

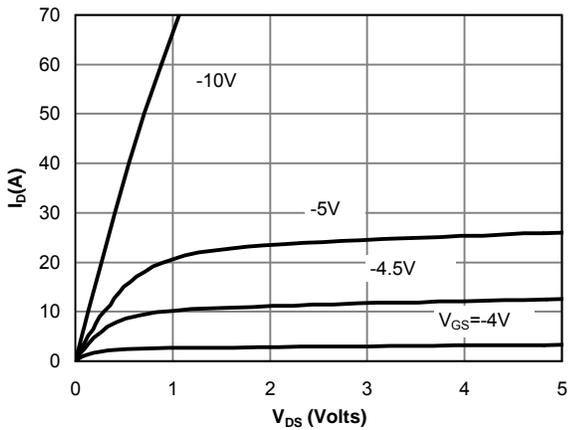


Figure 1: On-Region Characteristics

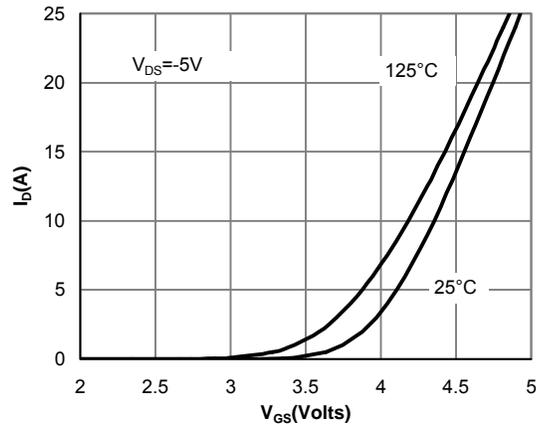


Figure 2: Transfer Characteristics

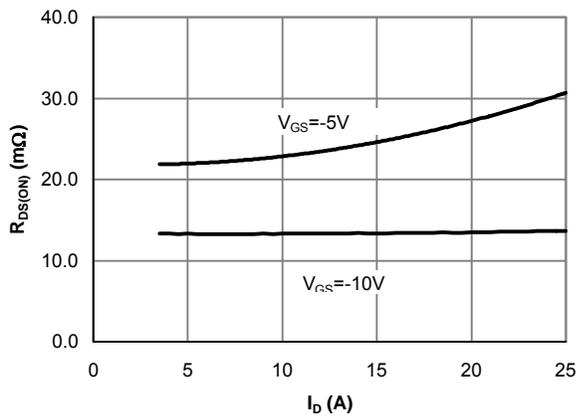


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

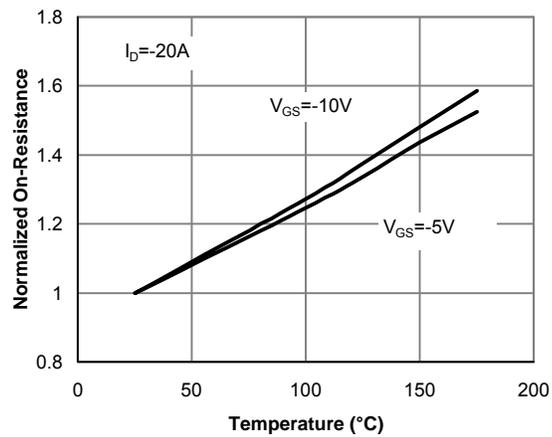


Figure 4: On-Resistance vs. Junction Temperature

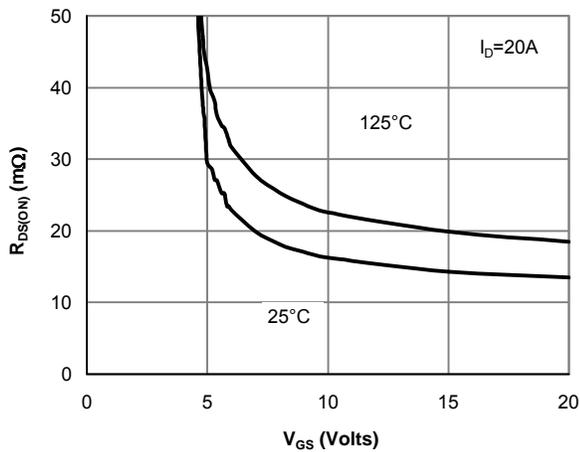


Figure 5: On-Resistance vs. Gate-Source Voltage

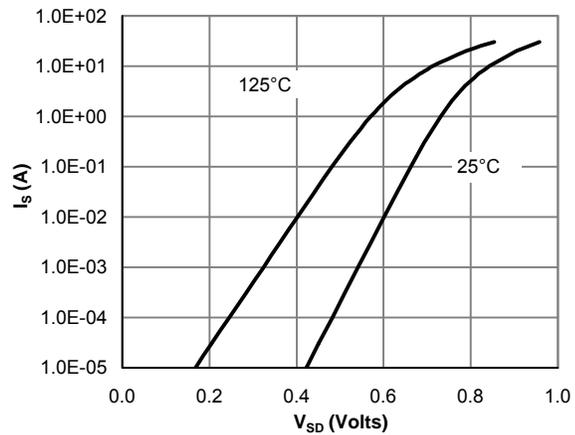


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

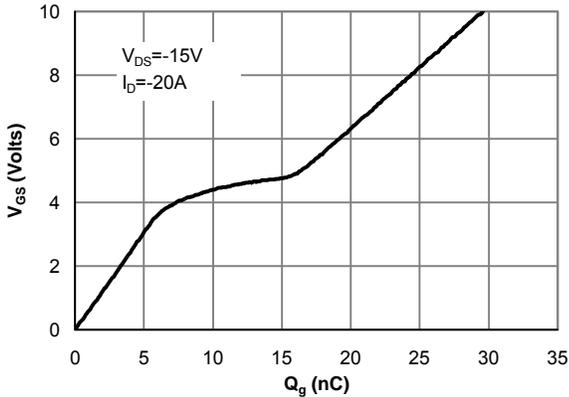


Figure 7: Gate-Charge Characteristics

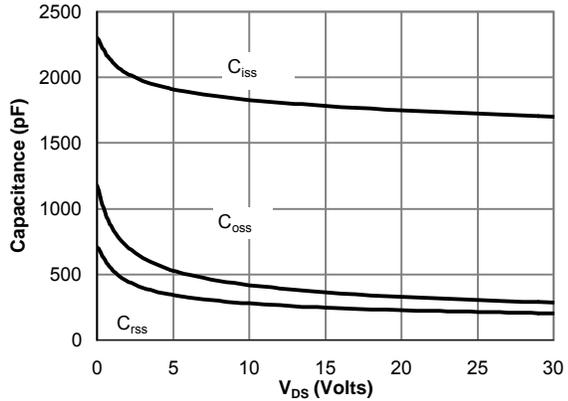


Figure 8: Capacitance Characteristics

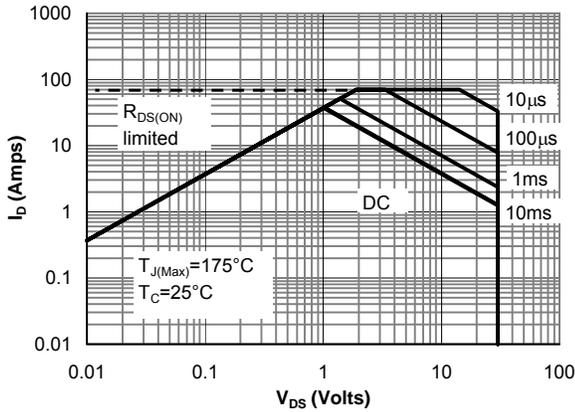


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

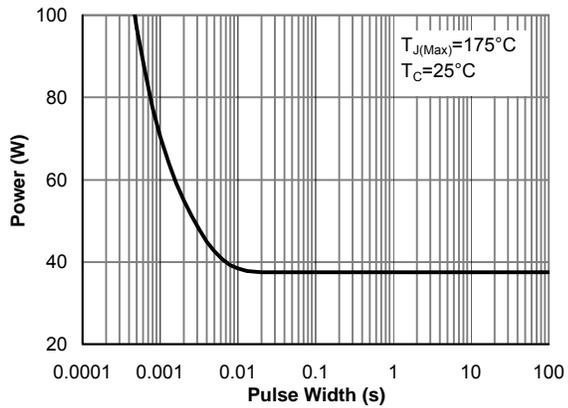


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

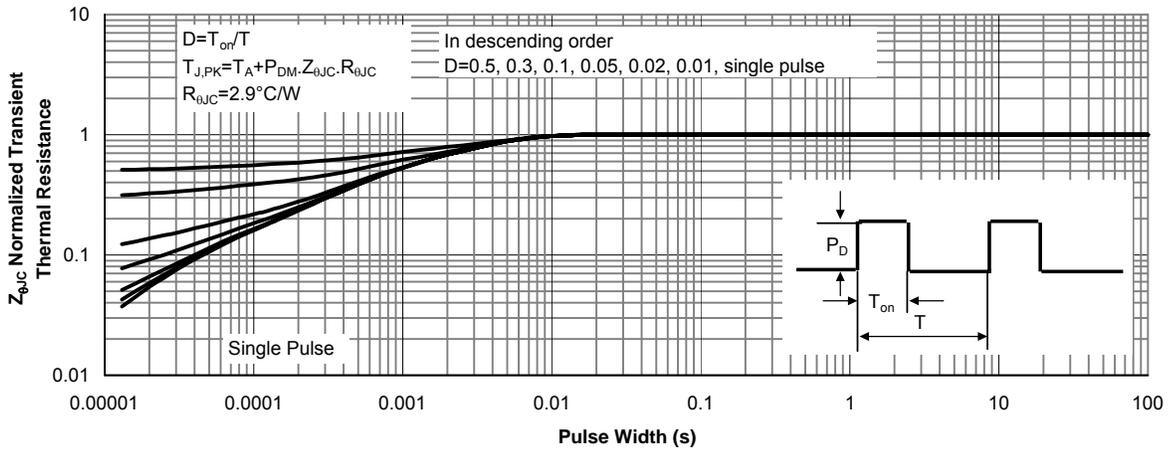


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

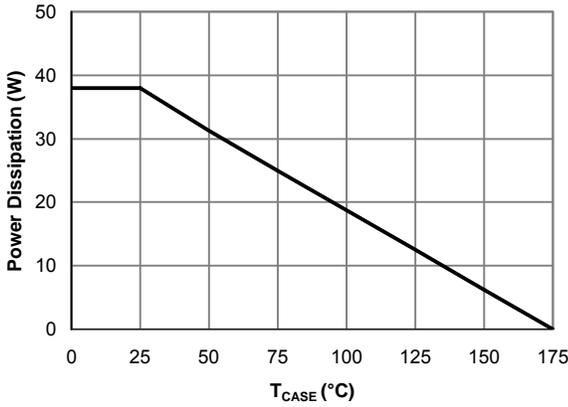


Figure 13: Power De-rating (Note B)

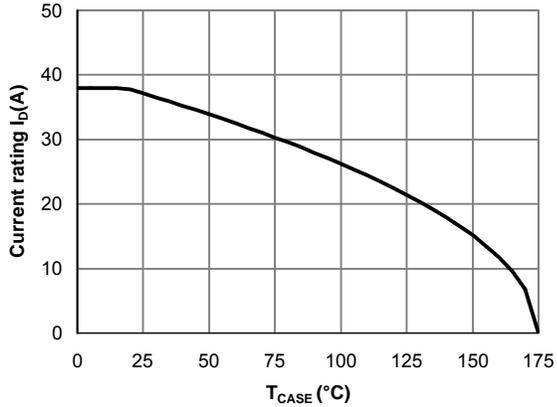


Figure 14: Current De-rating (Note B)

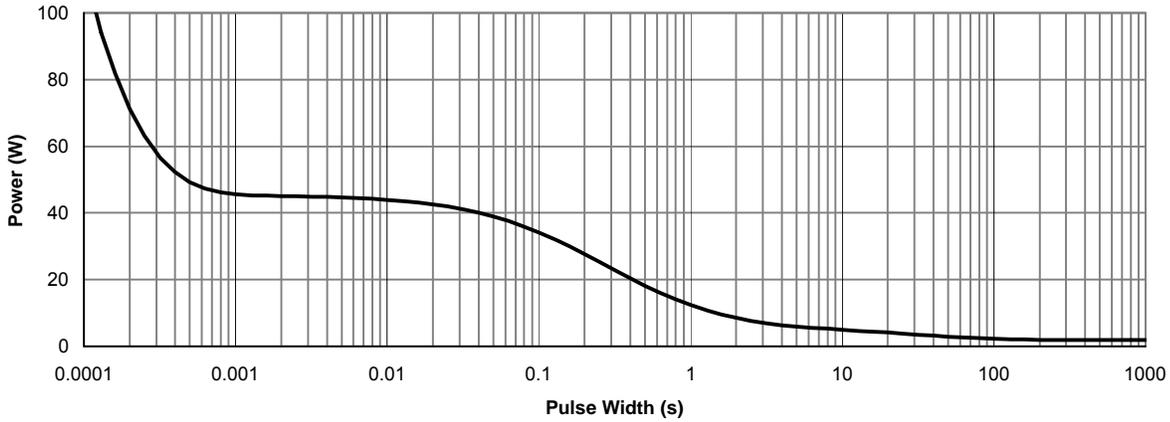


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

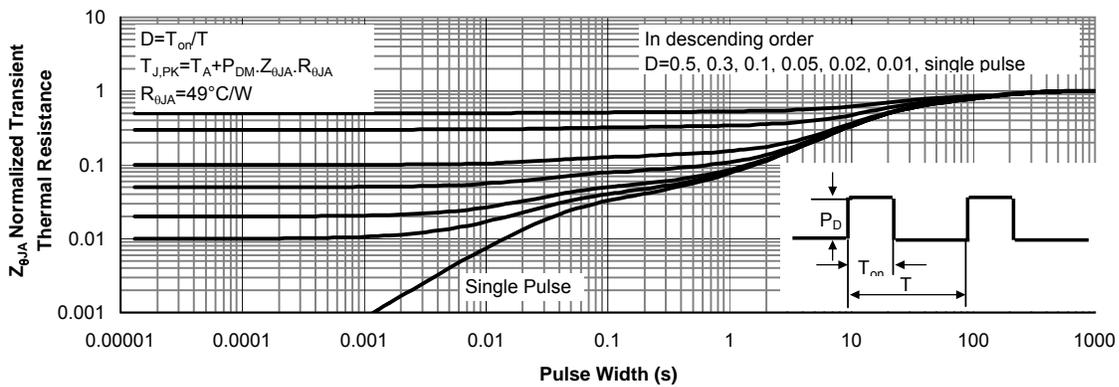


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)