ALPHA & OMEGA
SEMICONDUCTOR

AOL1412
N-Channel Enhancement Mode Field Effect Transistor
SRFET ™

General Description

SRFET^{TM} AOL1412 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$,and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications.
Standard Product AOL1412 is Pb-free (meets ROHS & Sony 259 specifications).

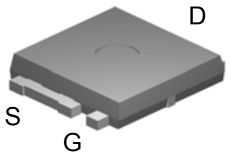
Features

V_{DS} (V) = 30V
I_D =85A (V_{GS} = 10V)
$R_{DS(ON)}$ < 3.9mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 4.6mΩ (V_{GS} = 4.5V)

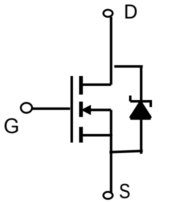
UIS Tested
Rg,Ciss,Coss,Crss Tested

Ultra SO-8^{TM} Top View

Fits SOIC8 footprint !



Bottom tab connected to drain



SRFET^{TM}
Soft **R**ecovery MOS**FET**:
Integrated Schottky Diode

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current ^{B}	T_C=25°C ^{I}	I_D	85	A
	T_C=100°C		84	
Pulsed Drain Current		I_{DM}	200	
Continuous Drain Current ^{H}	T_A=25°C	I_{DSM}	27	A
	T_A=70°C		21	
Avalanche Current ^{C}		I_{AR}	40	A
Repetitive avalanche energy L=0.3mH ^{C}		E_{AR}	240	mJ
Power Dissipation ^{B}	T_C=25°C	P_D	100	W
	T_C=100°C		50	
Power Dissipation ^{A}	T_A=25°C	P_{DSM}	5	W
	T_A=70°C		3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient ^{A}	t ≤ 10s	$R_{\theta JA}$	19.6	25	°C/W
Maximum Junction-to-Ambient ^{A}	Steady-State		50	60	°C/W
Maximum Junction-to-Case ^{C}	Steady-State	$R_{\theta JC}$	1	1.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=1mA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.1	mA
		T_J=125°C		9	20	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±12V			0.1	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.4	1.8	2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	200			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		3.2	3.9	mΩ
		T_J=125°C		5.0	6.2	
		V_{GS}=4.5V, I_D=20A		3.8	4.6	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		112		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.4	0.5	V
I_S	Maximum Body-Diode Continuous Current				85	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		6430	7716	pF
C_{oss}	Output Capacitance			756		pF
C_{rss}	Reverse Transfer Capacitance			352	493	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.45	0.9	1.4	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	VGS=10V, VDS=15V, ID=20A		96	115	
Q_g(4.5V)	Total Gate Charge			44	53	nC
Q_{gs}	Gate Source Charge			17		nC
Q_{gd}	Gate Drain Charge			13		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		17.5		ns
t_r	Turn-On Rise Time			10		ns
$t_{D(off)}$	Turn-Off DelayTime			56		ns
t_f	Turn-Off Fall Time			10.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=300A/µs		20	25	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=300A/µs		26		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25°C. The power dissipation P_{DSM} and current rating I_{DSM} are based on $T_{J(MAX)}$=150°C, using t ≤ 10s junction-to-ambient thermal resistance.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.
G. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
H. Surface mounted on a 1 in 2 FR-4 board with 2oz. Copper.
I. The maximum current rating is limited by bond-wires.
Rev 3:Dec 2006

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

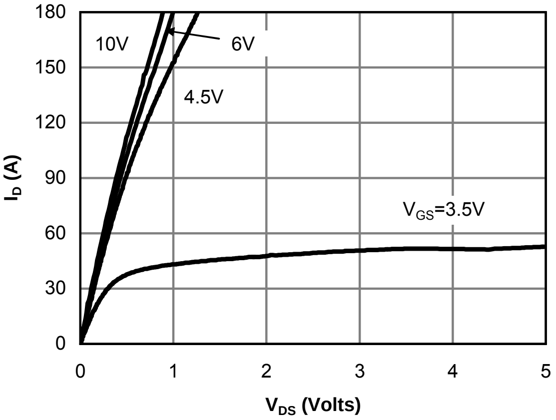


Figure 1: On-Region Characteristics

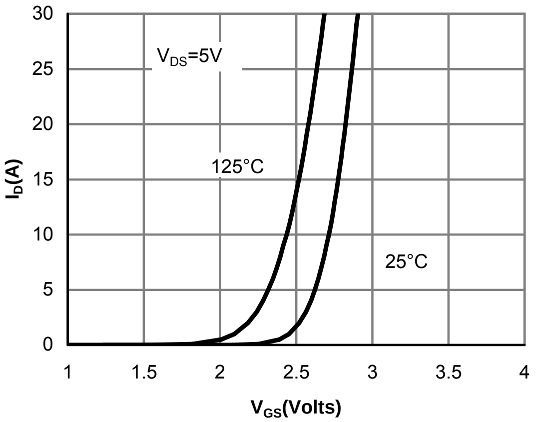


Figure 2: Transfer Characteristics

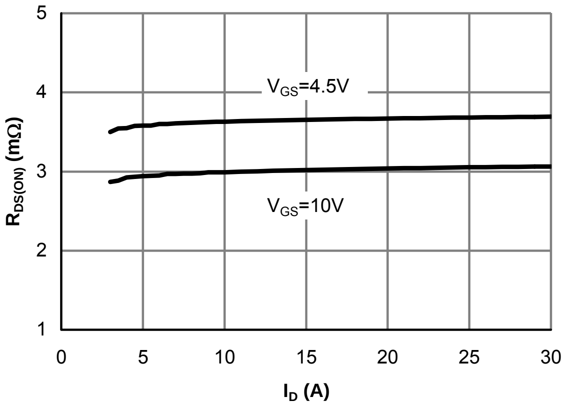


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

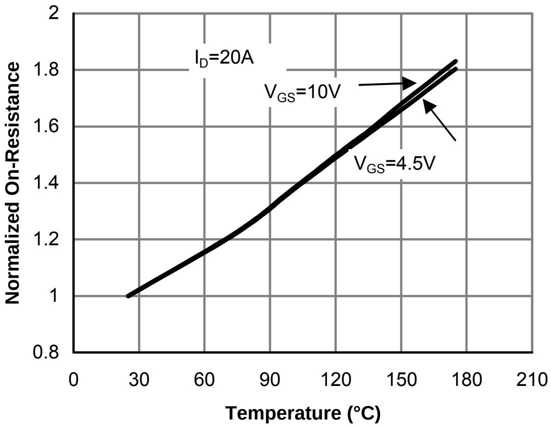


Figure 4: On-Resistance vs. Junction Temperature

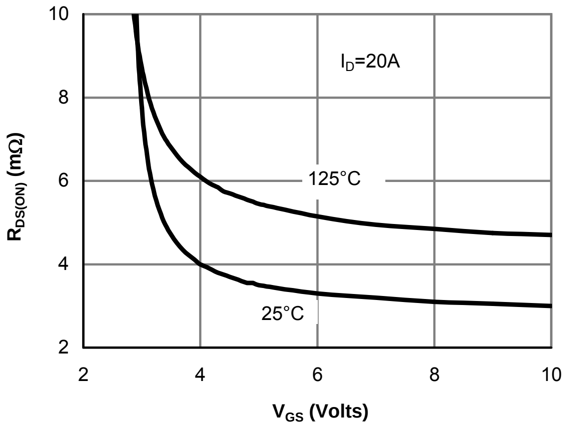


Figure 5: On-Resistance vs. Gate-Source Voltage

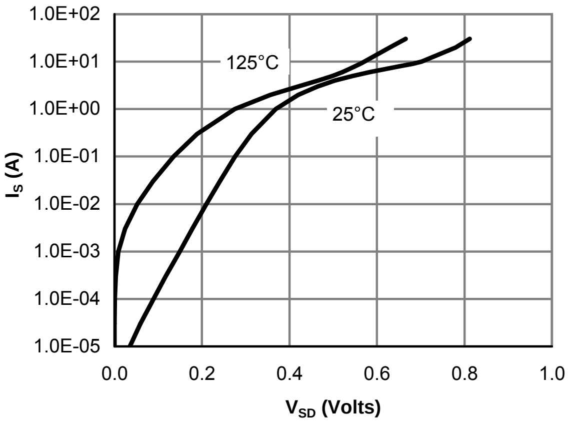


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

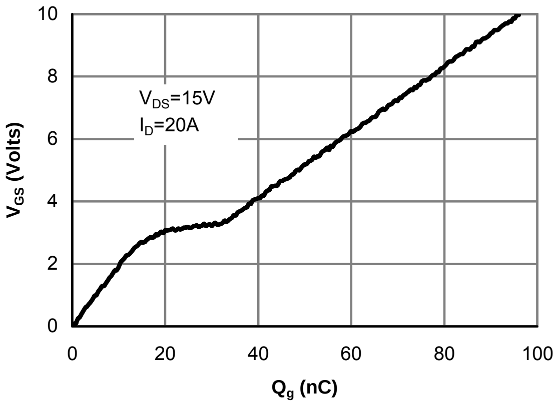


Figure 7: Gate-Charge Characteristics

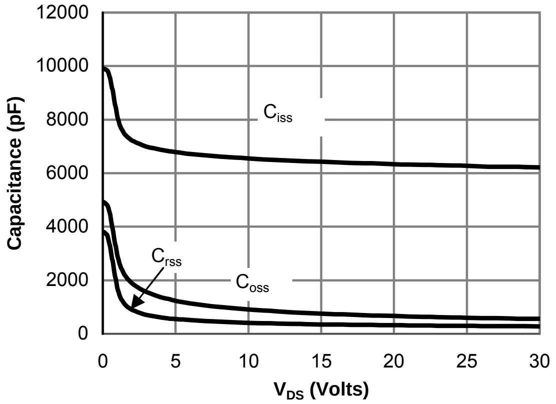


Figure 8: Capacitance Characteristics

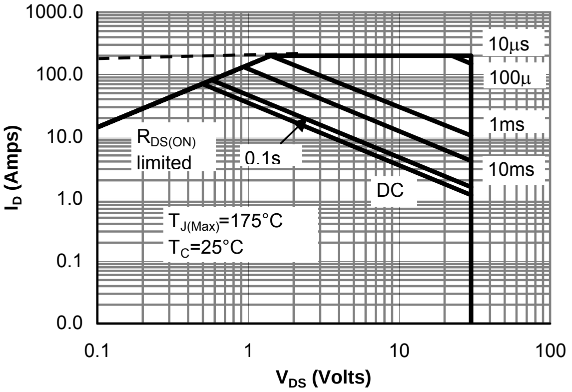


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

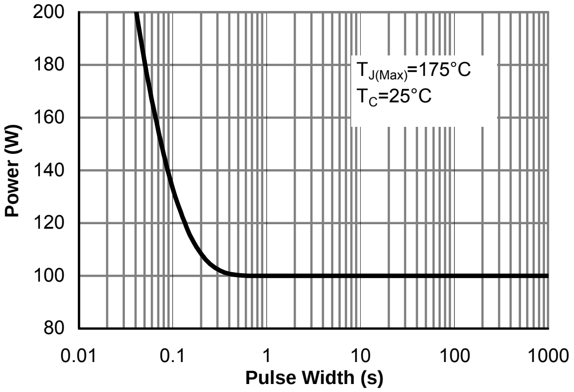


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

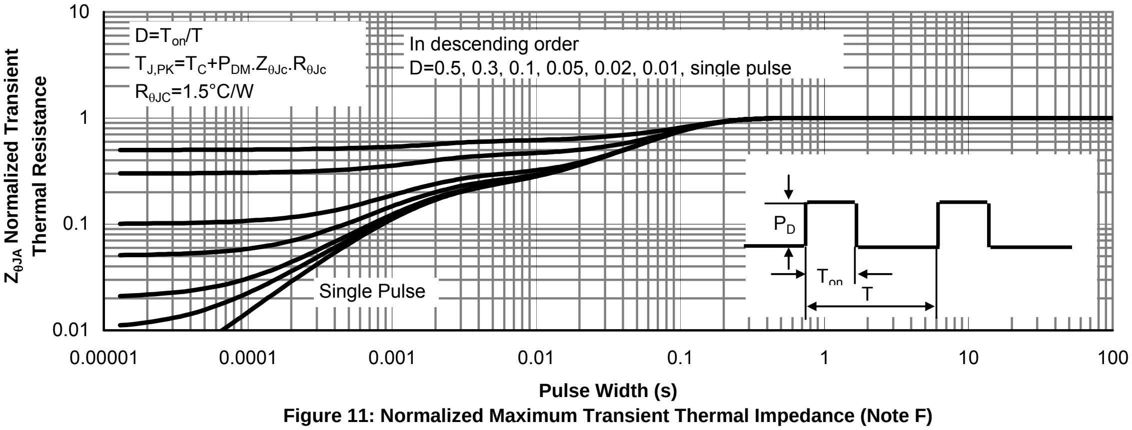


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

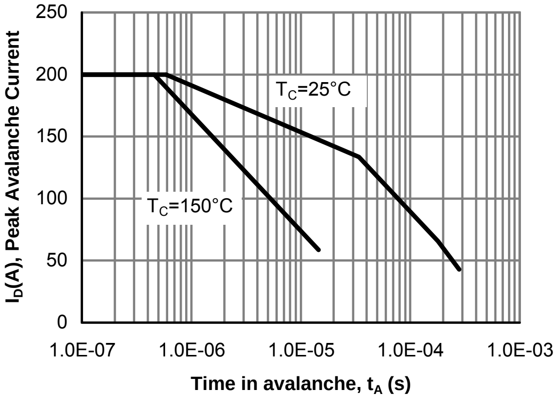


Figure 12: Single Pulse Avalanche capability

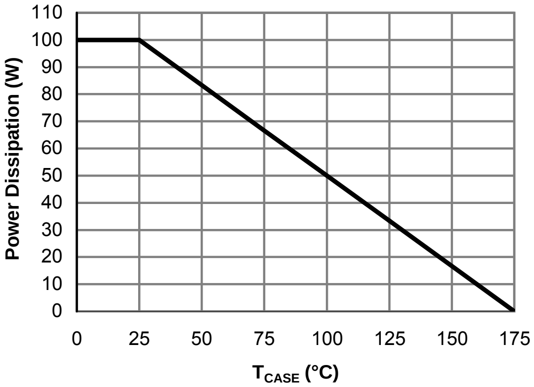


Figure 13: Power De-rating (Note B)

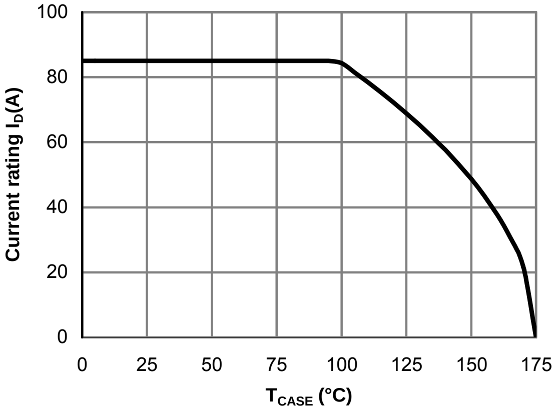


Figure 14: Current De-rating (Note B)

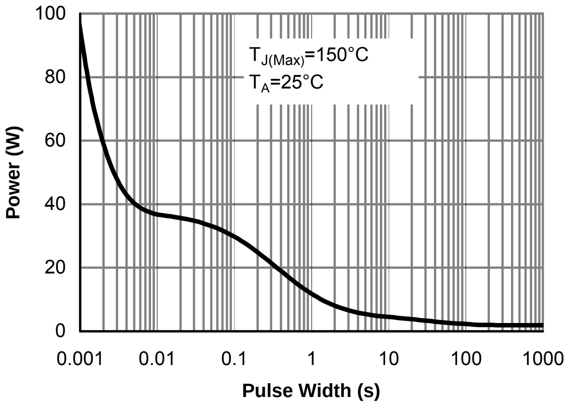


Figure15: Single Pulse Power Rating Junction-to-Ambient (Note G)

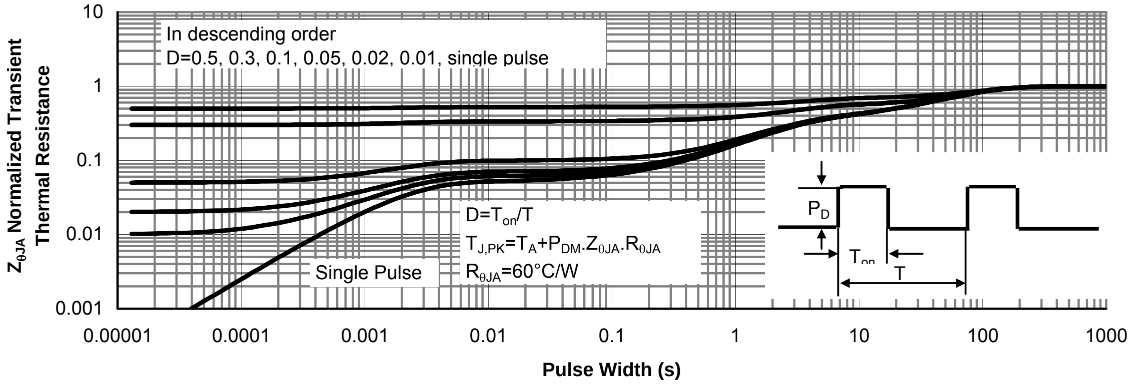


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

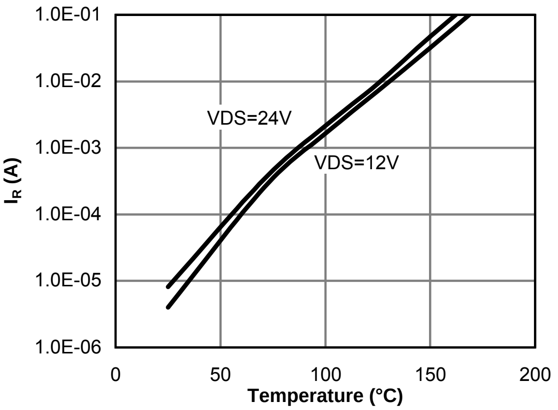


Figure 17: Diode Reverse Leakage Current vs. Junction Temperature

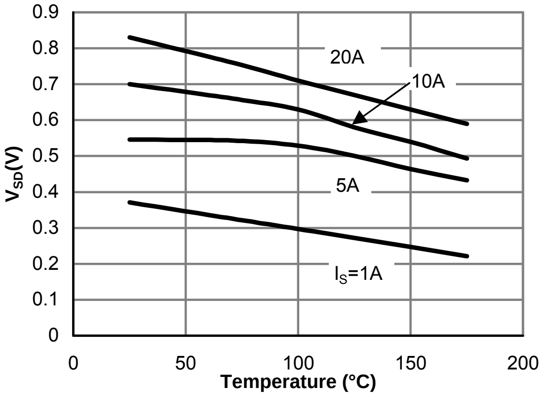


Figure 18: Diode Forward voltage vs. Junction Temperature

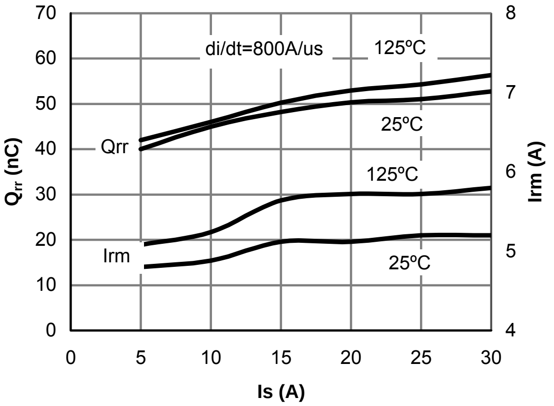


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

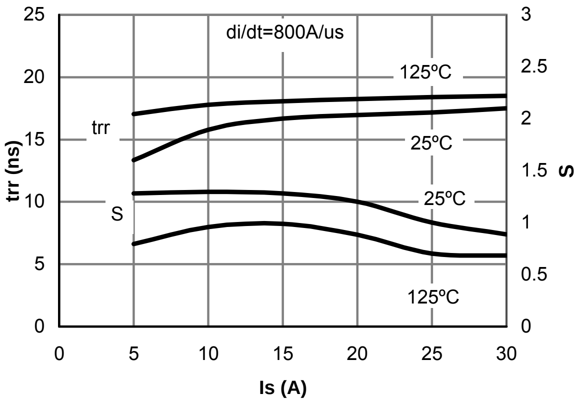


Figure 20: Diode Reverse Recovery Time and Soft Coefficient vs. Conduction Current

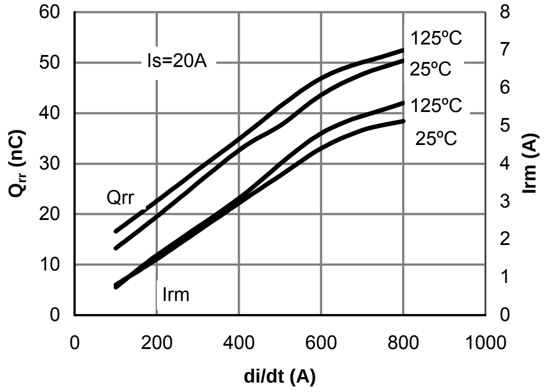


Figure 21: Diode Reverse Recovery Charge and Peak Current vs. di/dt

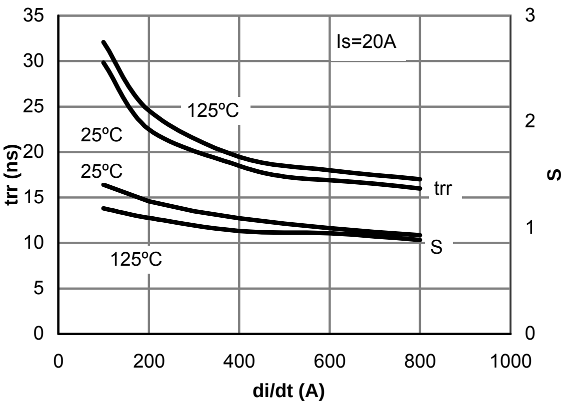


Figure 22: Diode Reverse Recovery Time and Soft Coefficient vs. di/dt