

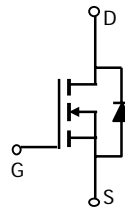
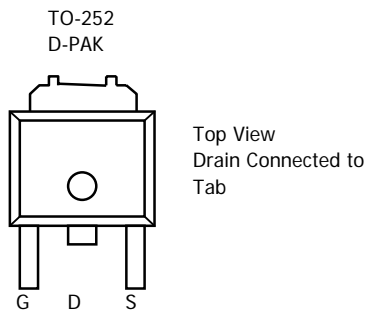
AOD488
N-Channel Enhancement Mode Field Effect Transistor

General Description

The AOD488 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications. *Standard Product AOD488 is Pb-free (meets ROHS & Sony 259 specifications). AOD488L is a Green Product ordering option. AOD488 and AOD488L are electrically identical.*

Features

V_{DS} (V) = 40V
 I_D = 20 A (V_{GS} = 10V)
 $R_{DS(ON)}$ < 26 m Ω (V_{GS} = 10V)
 $R_{DS(ON)}$ < 39 m Ω (V_{GS} = 4.5V)


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	20
		$T_C=100^\circ\text{C}$	15
Pulsed Drain Current ^C	I_{DM}	50	A
Avalanche Current ^C	I_{AR}	12	A
Repetitive avalanche energy $L=0.3\text{mH}$ ^C	E_{AR}	22	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	20
		$T_C=100^\circ\text{C}$	10
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	2
		$T_A=70^\circ\text{C}$	1.3
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$	17.4	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	50	$^\circ\text{C/W}$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	4	7.5	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	40	45		V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =32V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			0.1	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	2.3	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	50			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A		21.5	26	mΩ
		T _J =125°C		34	41	
		V _{GS} =4.5V, I _D =8A		31	39	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		25		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.76	1	V
I _S	Maximum Body-Diode Continuous Current				20	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz		404	500	pF
C _{oss}	Output Capacitance			95		pF
C _{rss}	Reverse Transfer Capacitance			37		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		2.7	4	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A		9.2	12	nC
Q _g (4.5V)	Total Gate Charge			4.5		nC
Q _{gs}	Gate Source Charge			1.6		nC
Q _{gd}	Gate Drain Charge			2.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =1.0Ω, R _{GEN} =3Ω		3.5		ns
t _r	Turn-On Rise Time			6		ns
t _{D(off)}	Turn-Off DelayTime			13.2		ns
t _f	Turn-Off Fall Time			3.5		ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =20A, dI/dt=100A/μs		22.9	
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=100A/μs		18.3		nC

A: The value of R_{qJA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{thJA} and the maximum allowed junction temperature of 150 °C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175 °C may be used if the PCB allows it.

B: The power dissipation PD is based on T_J(MAX)=175 °C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_J(MAX)=175 °C.

D: The R_{qJA} is the sum of the thermal impedance from junction to case R_{qJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_J(MAX)=175 °C.

G: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25 °C. The SOA curve provides a single pulse rating.

Rev 0: Mar. 2006

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

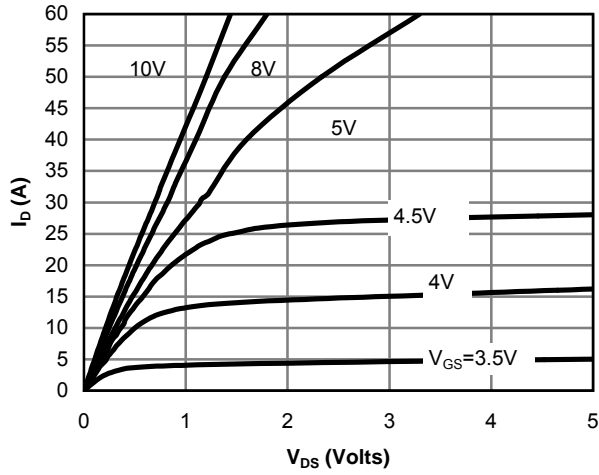


Fig 1: On-Region Characteristics

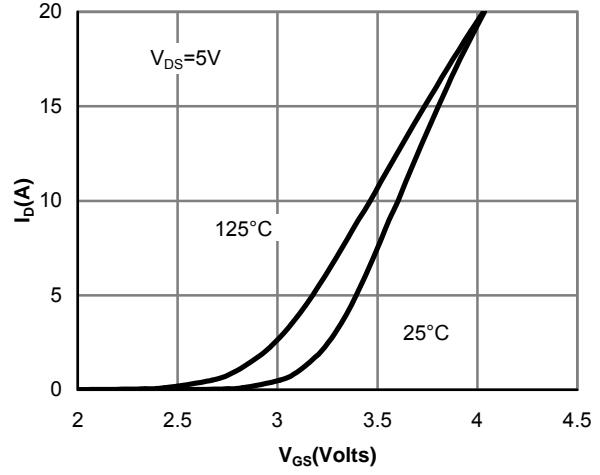


Figure 2: Transfer Characteristics

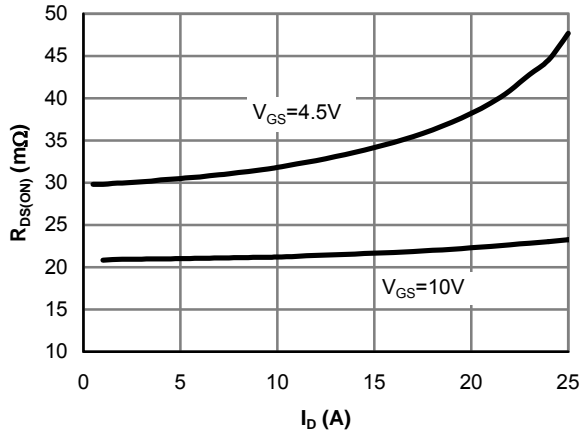


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

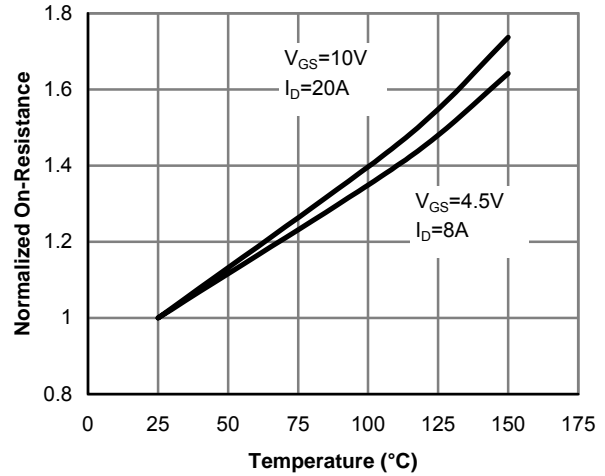


Figure 4: On-Resistance vs. Junction Temperature

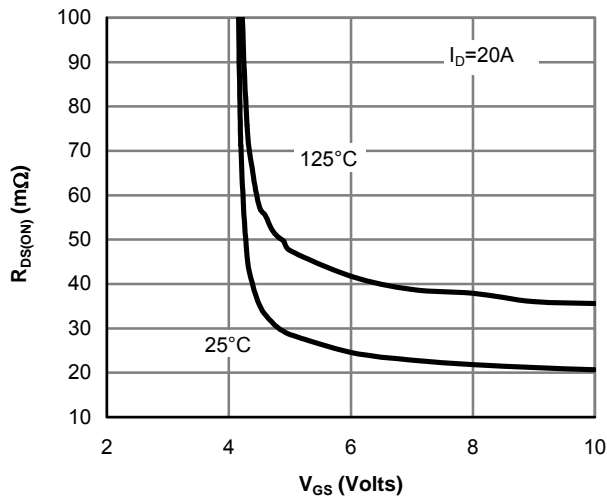


Figure 5: On-Resistance vs. Gate-Source Voltage

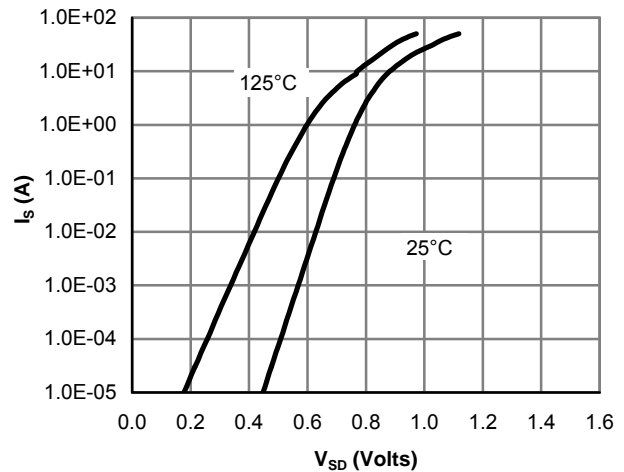


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

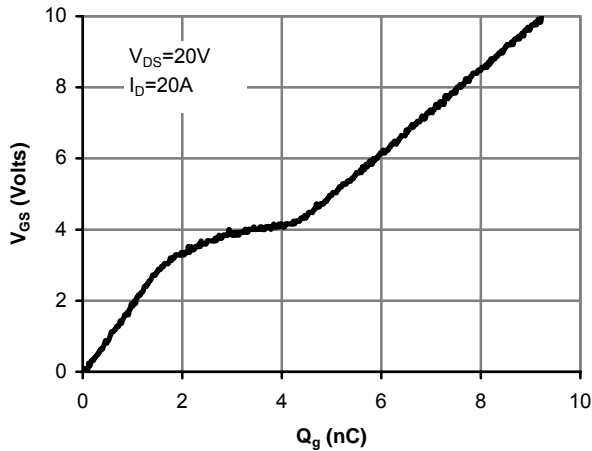


Figure 7: Gate-Charge Characteristics

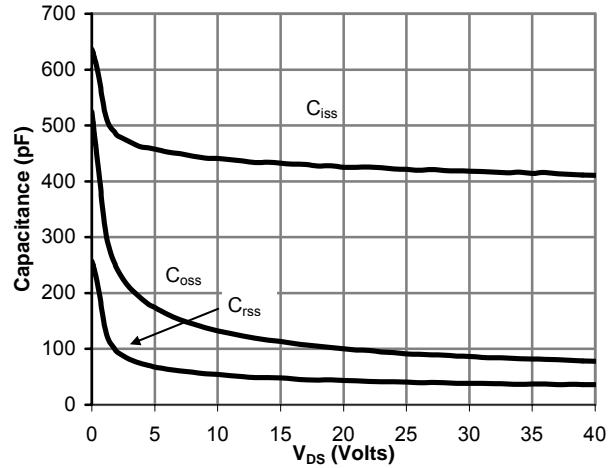


Figure 8: Capacitance Characteristics

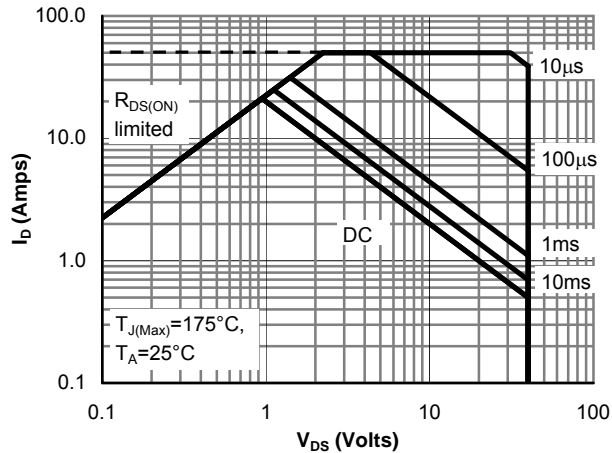


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

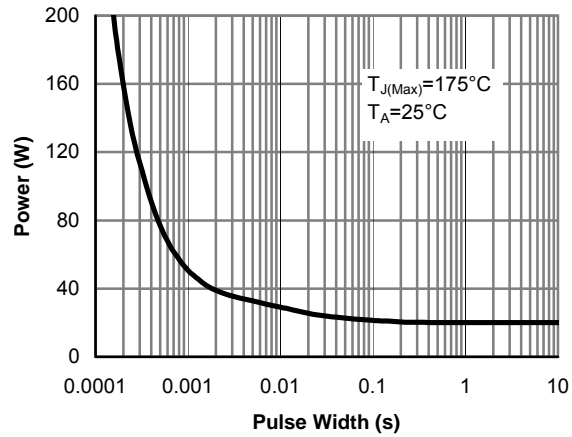


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

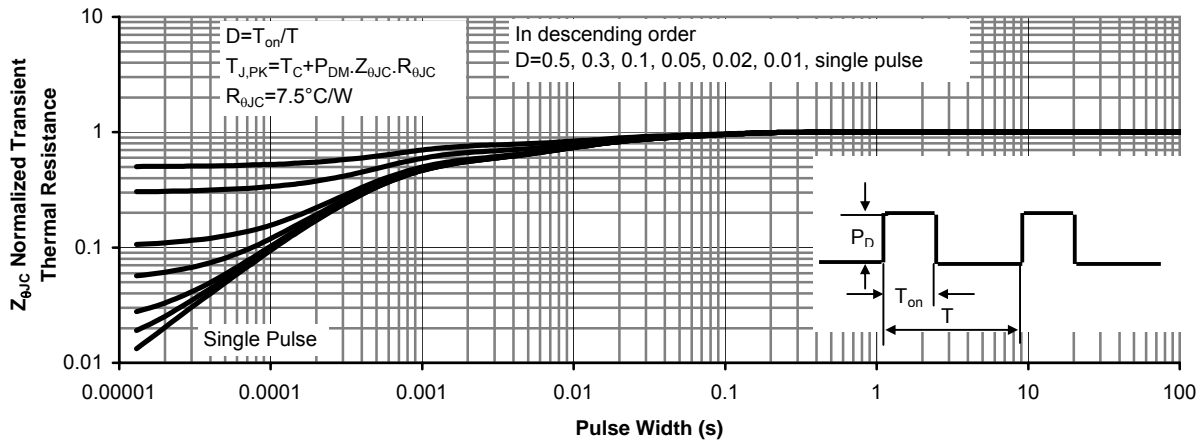


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

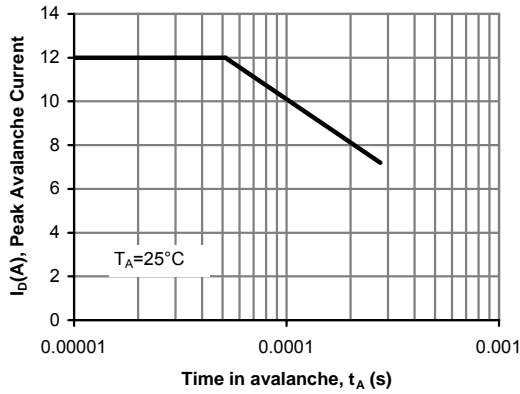


Figure 12: Single Pulse Avalanche capability

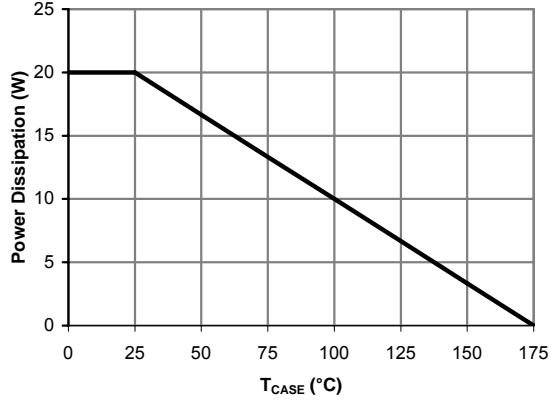


Figure 13: Power De-rating (Note B)

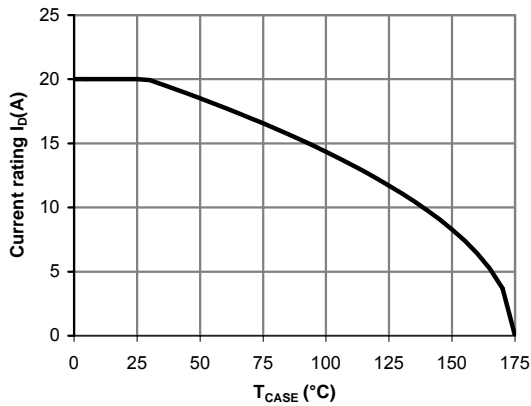


Figure 14: Current De-rating (Note B)

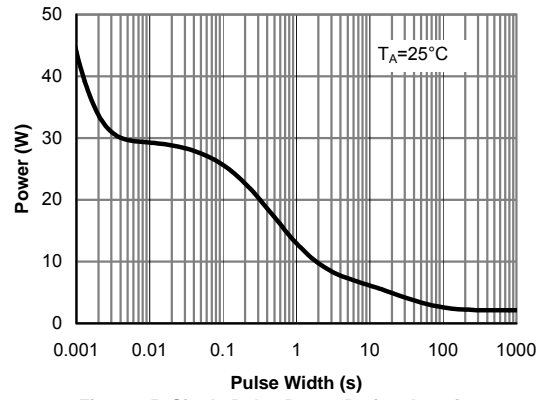


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

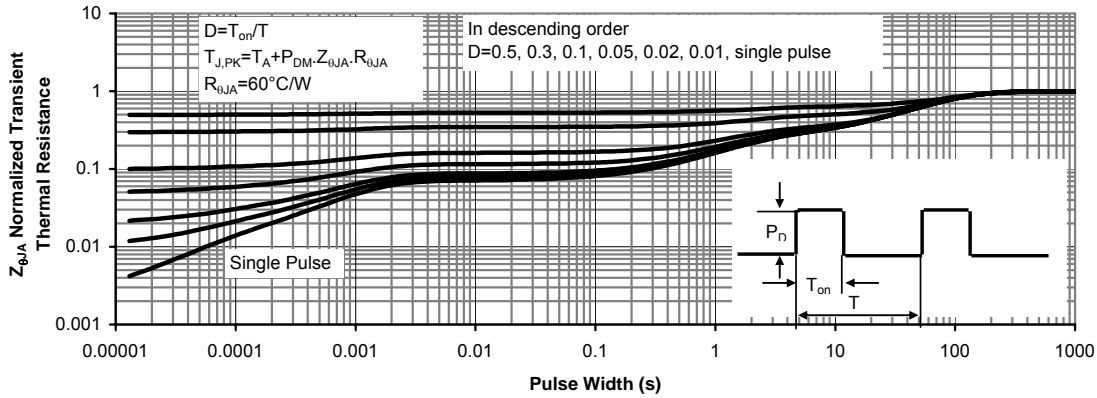


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)