ALPHA & OMEGA SEMICONDUCTOR

AOD421
P-Channel Enhancement Mode Field Effect Transistor

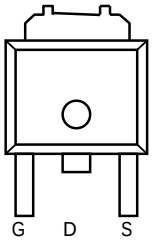
General Description

The AOD421 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for load switching. It is ESD protected. *Standard Product AOD421 is Pb-free (meets ROHS & Sony 259 specifications). AOD421L is a Green Product ordering option. AOD421 and AOD421L are electrically identical.*

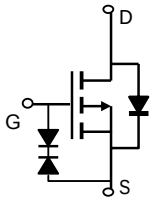
Features

V_{DS} (V) = -20V
I_D = -12.5 A (V_{GS} = -10V)
$R_{DS(ON)}$ < 75mΩ (V_{GS} = -10V)
$R_{DS(ON)}$ < 95mΩ (V_{GS} = -4.5V)
$R_{DS(ON)}$ < 145mΩ (V_{GS} = -2.5V)
ESD Rating: 2000V HBM

TO-252
D-PAK



Top View
Drain Connected
to Tab



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [G]	T_A=25°C	I_D	-12.5	A
	T_A=70°C		-8.9	
Pulsed Drain Current [C]		I_{DM}	-30	
Power Dissipation [B]	T_C=25°C	P_D	18.8	W
	T_C=100°C		9.4	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2	W
	T_A=70°C		1.33	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	23	28	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		50	60	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	6	8	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-16V, V_{GS}=0V			-0.5	µA
		T_J=55°C			-2.5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±10V			±1	µA
		V_{DS}=0V, V_{GS}=±12V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-0.7	-0.9	-1.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=-4.5V, V_{DS}=-5V	-15			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-12.5A		61	75	mΩ
		T_J=125°C		83	105	
		V_{GS}=-4.5V, I_D=-3A		75	95	mΩ
		V_{GS}=-2.5V, I_D=-1A		110	145	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-12.5A		8.8		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V	-1	-0.81		V
I_S	Maximum Body-Diode Continuous Current				-8.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-10V, f=1MHz		512	620	pF
C_{oss}	Output Capacitance			77		pF
C_{rss}	Reverse Transfer Capacitance			62		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		9.2	13	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-4.5V, V_{DS}=-10V, I_D=-12.5A		4.6		nC
Q_{gs}	Gate Source Charge			0.9		nC
Q_{gd}	Gate Drain Charge			2.1		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-10V, R_L=0.75Ω, R_{GEN}=3Ω		5.2		ns
t_r	Turn-On Rise Time			38		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			31		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-12.5A, dI/dt=100A/µs		19		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-12.5A, dI/dt=100A/µs		6.3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

I. Revision 0: July 2006

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

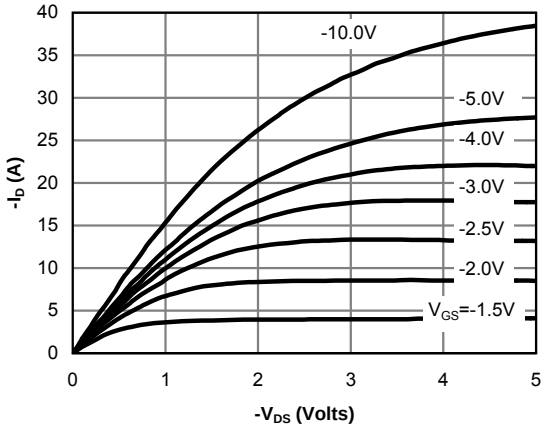


Figure 1: On-Region Characteristics

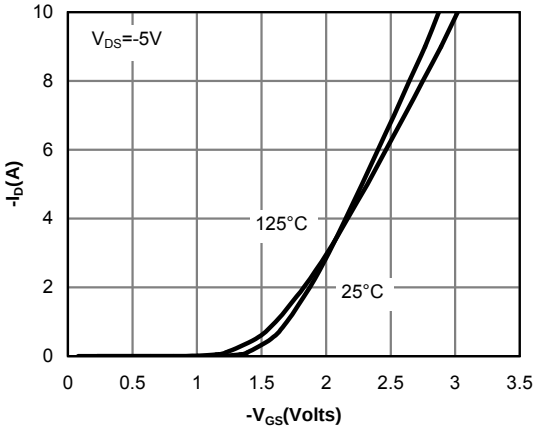


Figure 2: Transfer Characteristics

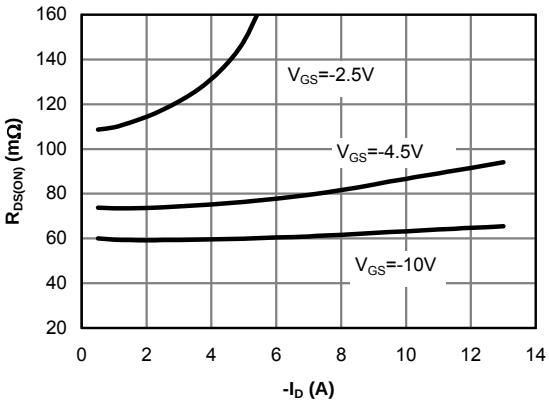


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

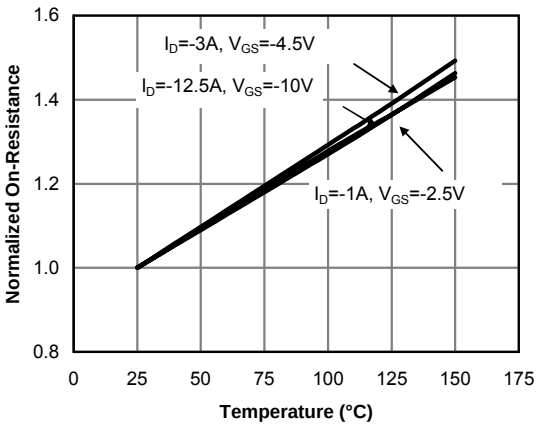


Figure 4: On-Resistance vs. Junction Temperature

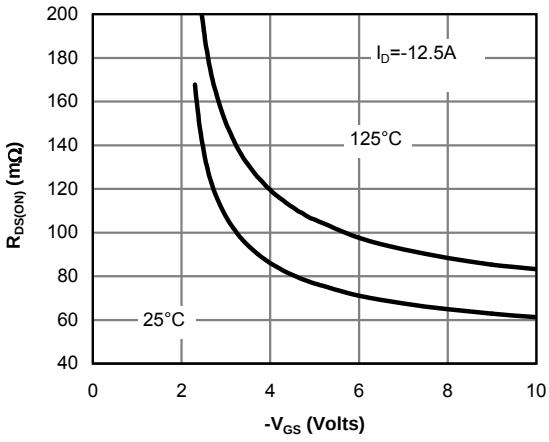


Figure 5: On-Resistance vs. Gate-Source Voltage

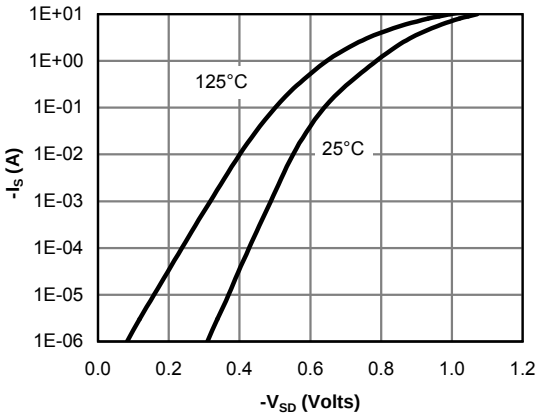


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

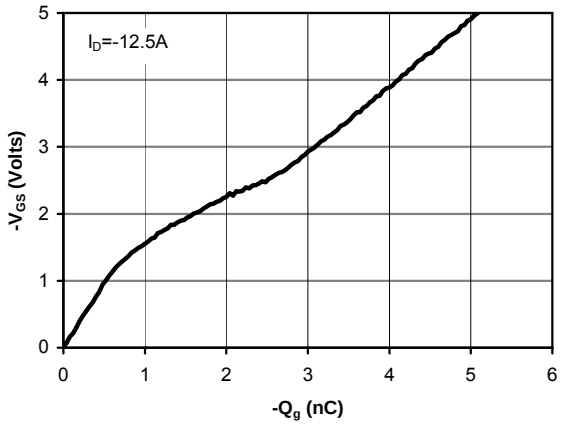


Figure 7: Gate-Charge Characteristics

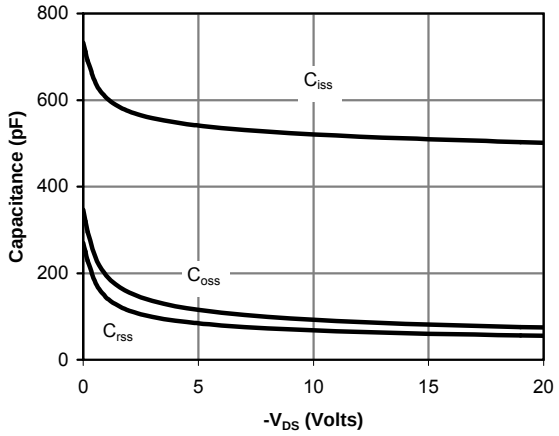


Figure 8: Capacitance Characteristics

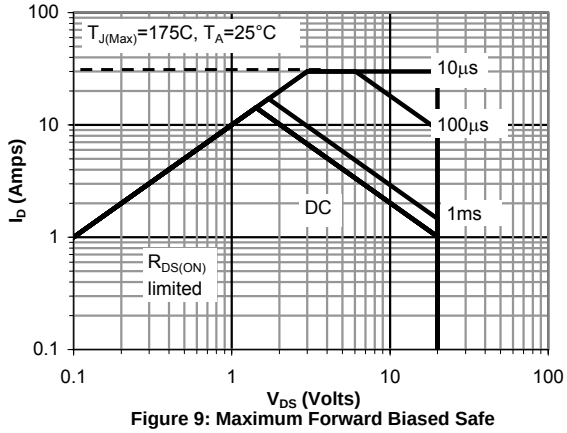


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

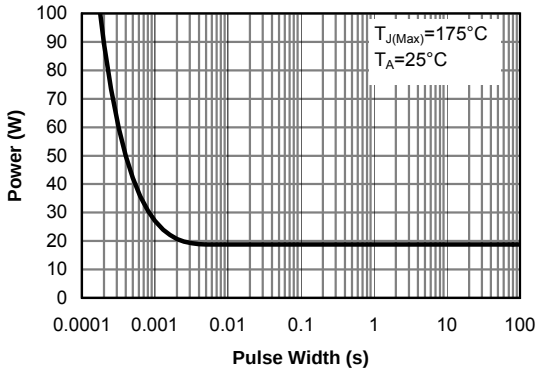


Figure 10: Single Pulse Power Rating Junction-to-case (Note F)

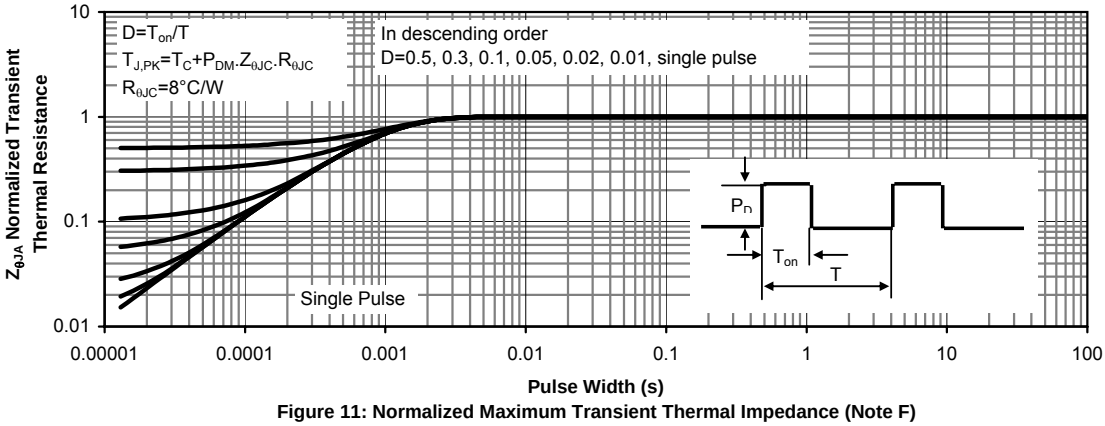


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

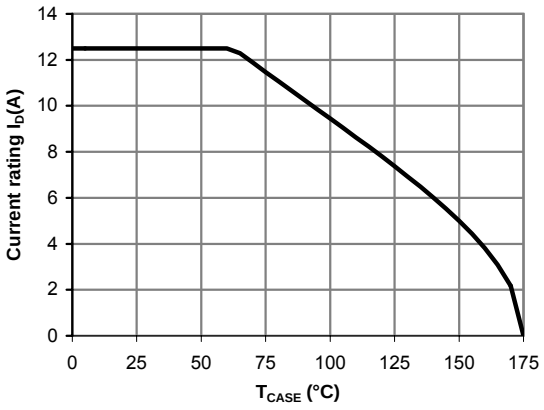


Figure 12: Current De-rating (Note B)

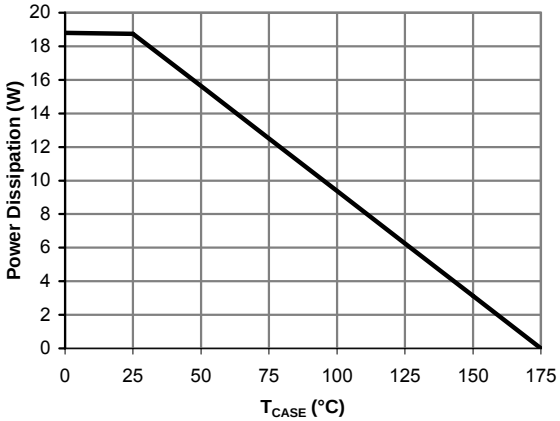


Figure 13: Power De-rating (Note B)

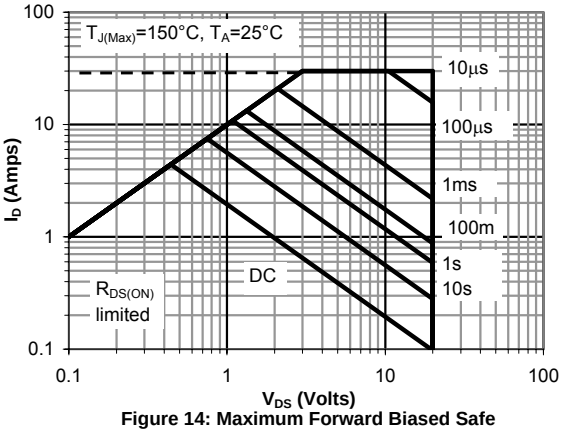


Figure 14: Maximum Forward Biased Safe Operating Area (Note H)

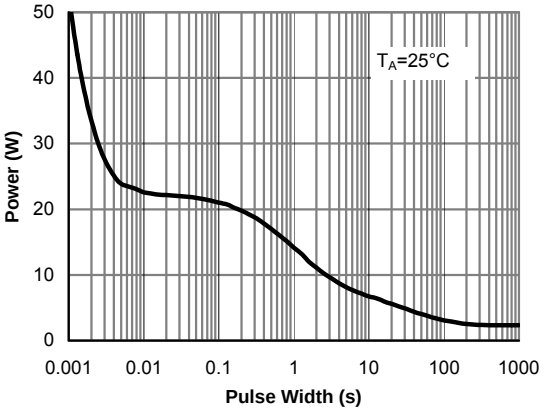


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

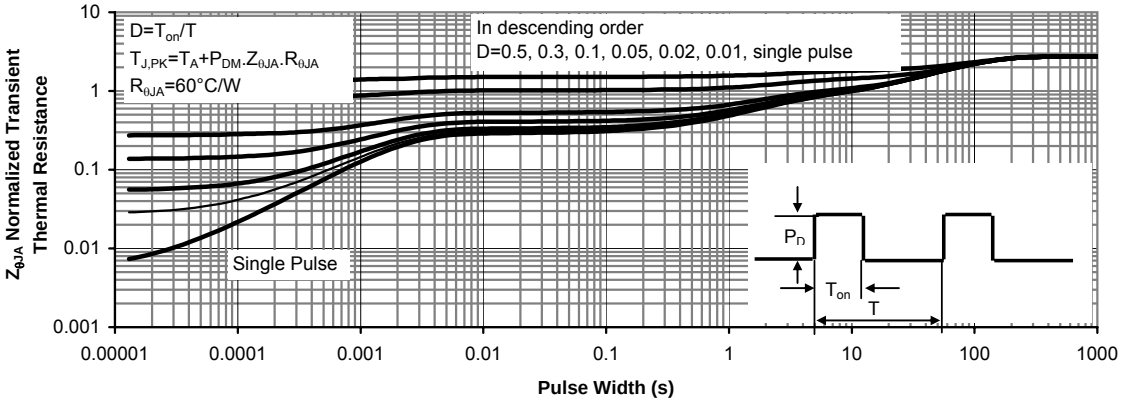


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)