

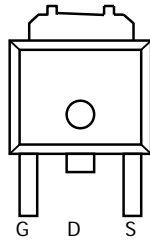
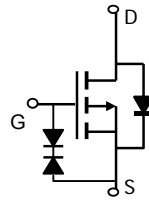
**AOD421**  
**P-Channel Enhancement Mode Field Effect Transistor**

**General Description**

The AOD421 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for load switching. It is ESD protected. *Standard Product AOD421 is Pb-free (meets ROHS & Sony 259 specifications). AOD421L is a Green Product ordering option. AOD421 and AOD421L are electrically identical.*

**Features**

$V_{DS}$  (V) = -20V  
 $I_D$  = -12.5 A ( $V_{GS}$  = -10V)  
 $R_{DS(ON)} < 75m\Omega$  ( $V_{GS}$  = -10V)  
 $R_{DS(ON)} < 95m\Omega$  ( $V_{GS}$  = -4.5V)  
 $R_{DS(ON)} < 145m\Omega$  ( $V_{GS}$  = -2.5V)  
 ESD Rating: 2000V HBM

 TO-252  
 D-PAK

 Top View  
 Drain Connected  
 to Tab

**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-30	
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

**Thermal Characteristics**

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$t \leq 10\text{s}$	$R_{\theta JA}$	23	28	$^\circ\text{C/W}$
	Steady-State		50	60	
Maximum Junction-to-Case <sup>B</sup>	Steady-State	$R_{\theta JC}$	6	8	$^\circ\text{C/W}$

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$ , $V_{GS}=0\text{V}$	-20			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-16\text{V}$ , $V_{GS}=0\text{V}$			-0.5	$\mu\text{A}$
		$T_J=55^\circ\text{C}$			-2.5	
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 10\text{V}$			$\pm 1$	$\mu\text{A}$
		$V_{DS}=0\text{V}$ , $V_{GS}=\pm 12\text{V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$	-0.7	-0.9	-1.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-4.5\text{V}$ , $V_{DS}=-5\text{V}$	-15			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$ , $I_D=-12.5\text{A}$		61	75	$\text{m}\Omega$
		$T_J=125^\circ\text{C}$		83	105	
		$V_{GS}=-4.5\text{V}$ , $I_D=-3\text{A}$		75	95	$\text{m}\Omega$
		$V_{GS}=-2.5\text{V}$ , $I_D=-1\text{A}$		110	145	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=-5\text{V}$ , $I_D=-12.5\text{A}$		8.8		S
$V_{SD}$	Diode Forward Voltage	$I_S=-1\text{A}$ , $V_{GS}=0\text{V}$	-1	-0.81		V
$I_S$	Maximum Body-Diode Continuous Current				-8.5	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance			512	620	pF
$C_{oss}$	Output Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=-10\text{V}$ , $f=1\text{MHz}$		77		pF
$C_{rss}$	Reverse Transfer Capacitance			62		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		9.2	13	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g$	Total Gate Charge	$V_{GS}=-4.5\text{V}$ , $V_{DS}=-10\text{V}$ , $I_D=-12.5\text{A}$		4.6		nC
$Q_{gs}$	Gate Source Charge			0.9		nC
$Q_{gd}$	Gate Drain Charge			2.1		nC
$t_{D(on)}$	Turn-On Delay Time			5.2		ns
$t_r$	Turn-On Rise Time	$V_{GS}=-10\text{V}$ , $V_{DS}=-10\text{V}$ , $R_L=0.75\Omega$ , $R_{GEN}=3\Omega$		38		ns
$t_{D(off)}$	Turn-Off Delay Time			17		ns
$t_f$	Turn-Off Fall Time			31		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=-12.5\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		19		ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=-12.5\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		6.3		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B: The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^\circ\text{C}$ .

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

I: Revision 0: July 2006

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

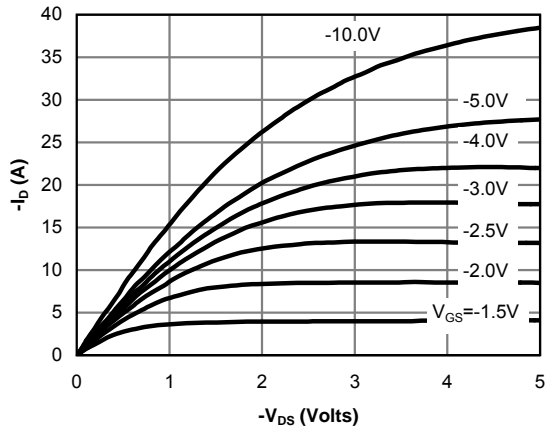


Figure 1: On-Region Characteristics

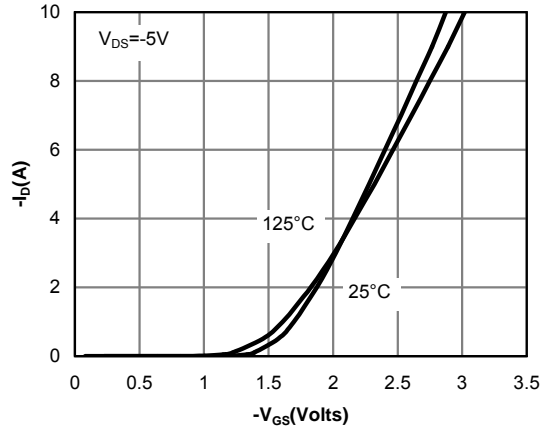


Figure 2: Transfer Characteristics

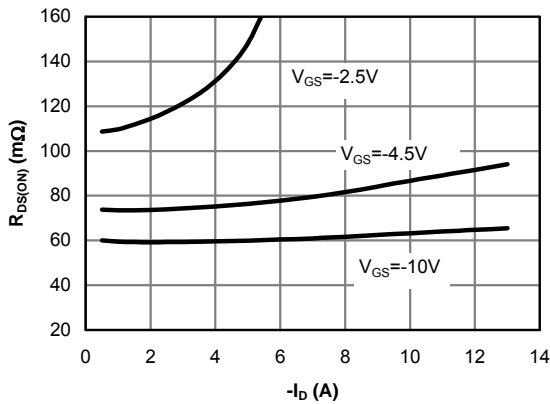


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

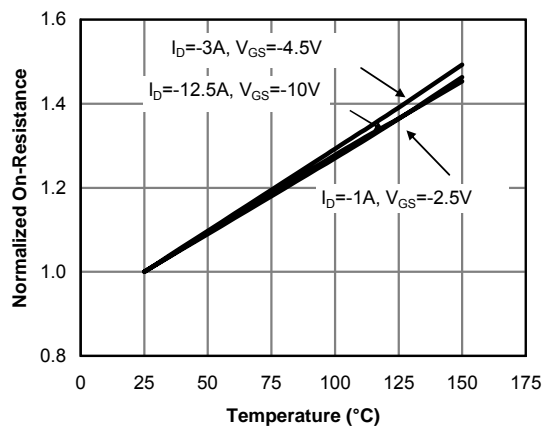


Figure 4: On-Resistance vs. Junction Temperature

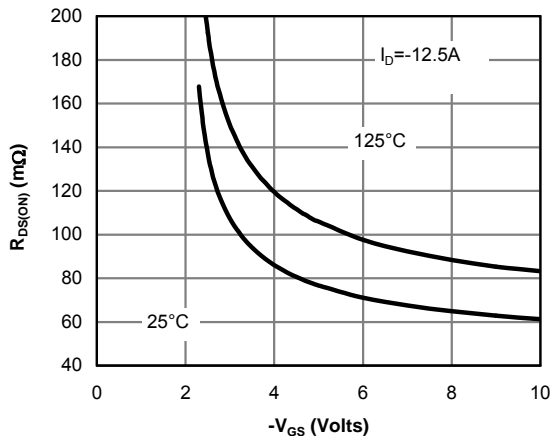


Figure 5: On-Resistance vs. Gate-Source Voltage

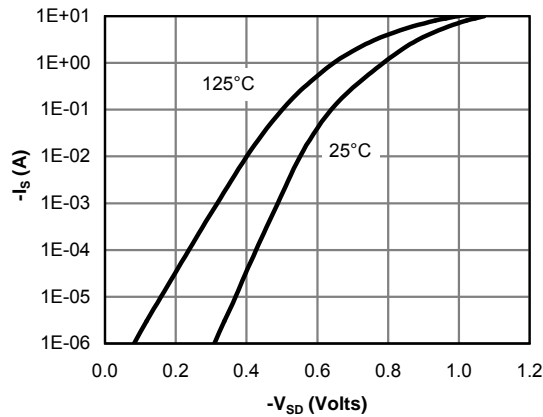


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

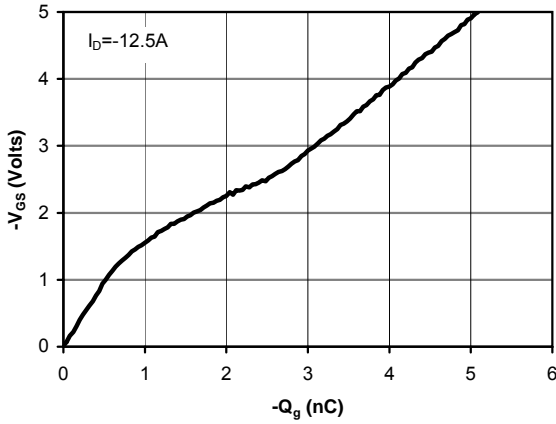


Figure 7: Gate-Charge Characteristics

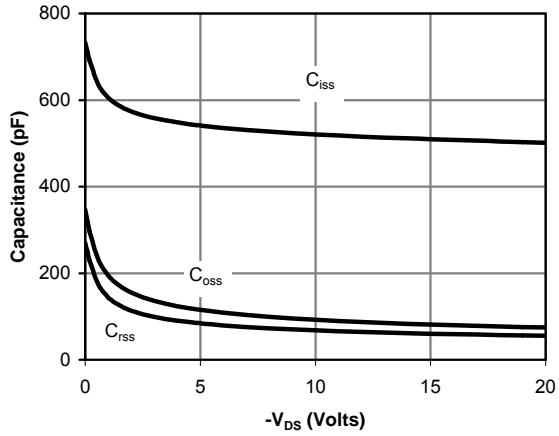


Figure 8: Capacitance Characteristics

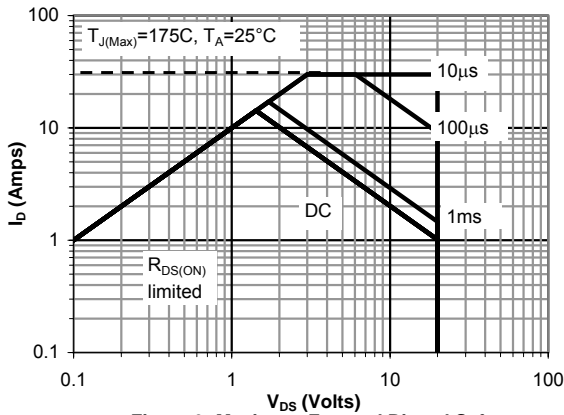


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

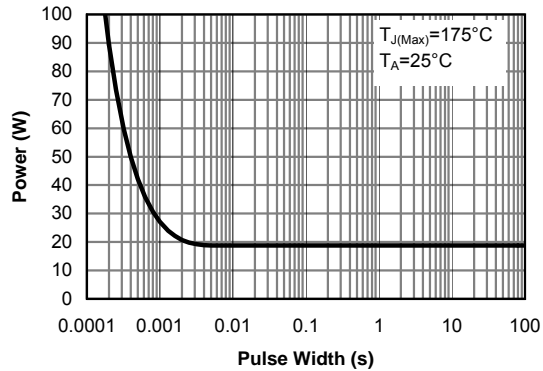


Figure 10: Single Pulse Power Rating Junction-to-case (Note F)

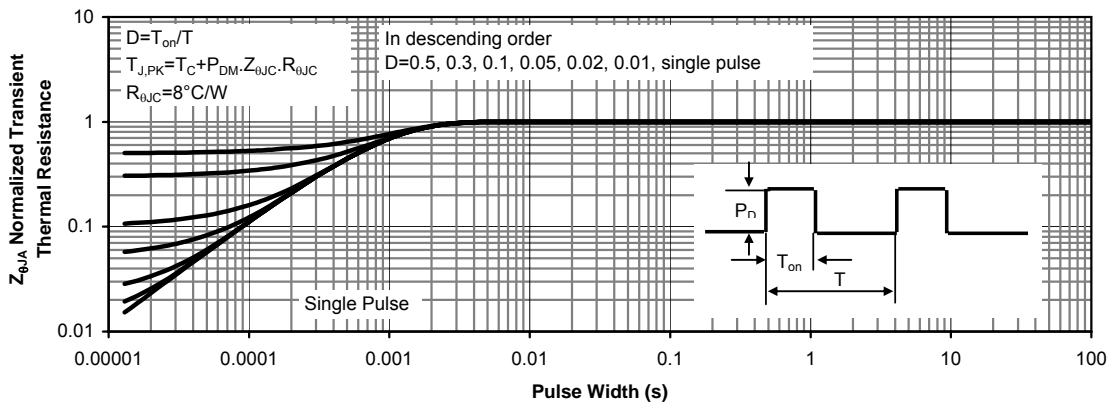


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

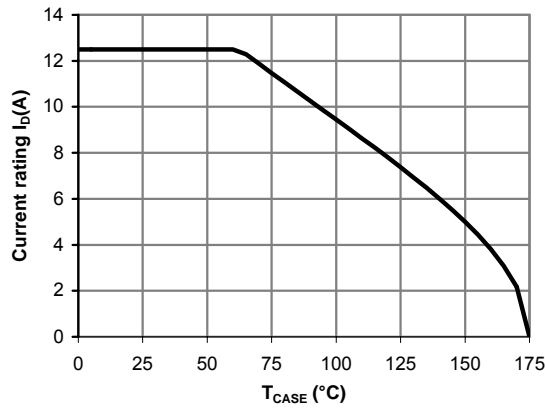


Figure 12: Current De-rating (Note B)

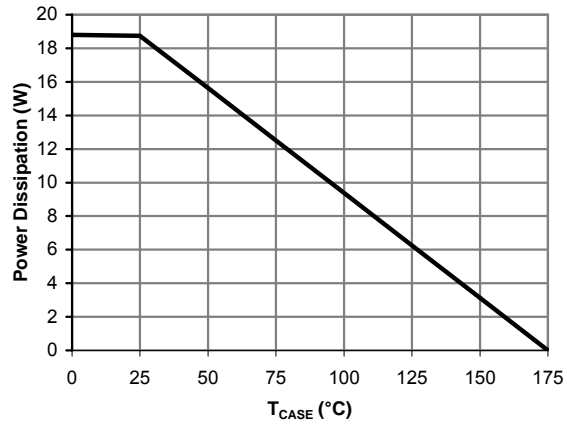


Figure 13: Power De-rating (Note B)

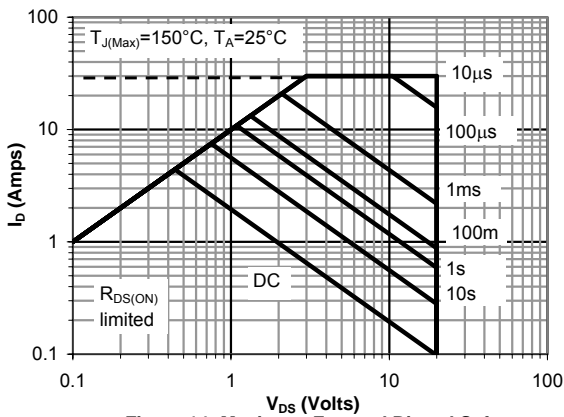


Figure 14: Maximum Forward Biased Safe Operating Area (Note H)

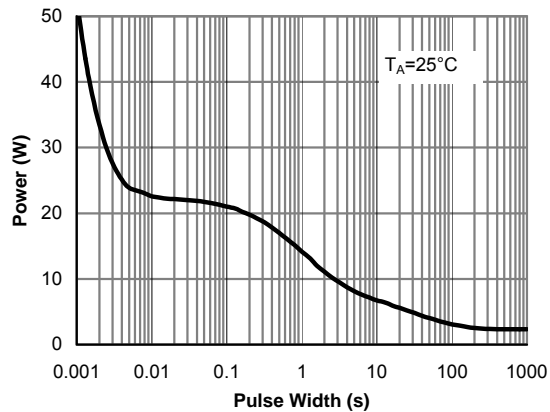


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

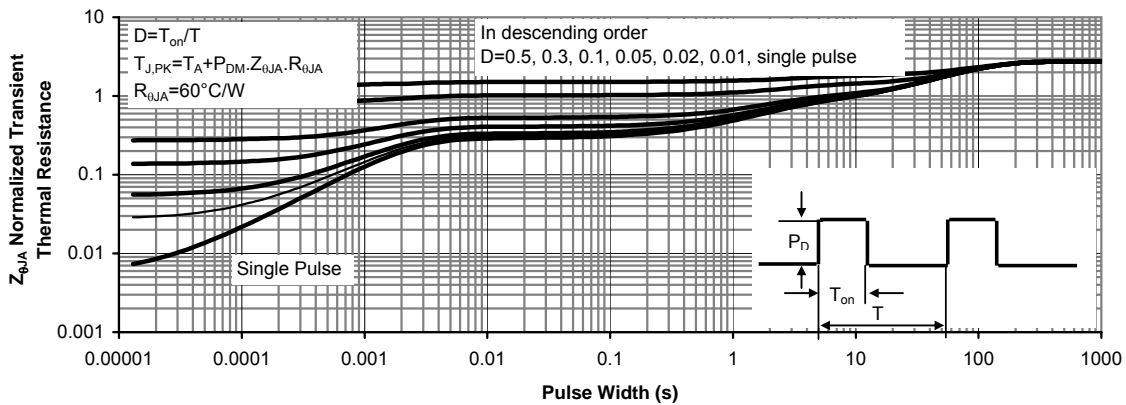


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)