



**AO4447**

**P-Channel Enhancement Mode Field Effect Transistor**

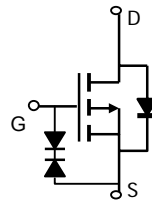
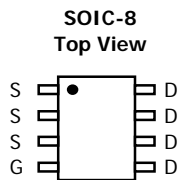
**General Description**

The AO4447 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , and ultra-low low gate charge. This device is suitable for use as a load switch. The device is ESD protected.  
*Standard Product AO4447 is Pb-free (meets ROHS & Sony 259 specifications).*

**Features**

$V_{DS}$  (V) = -30V  
 $I_D$  = -15 A ( $V_{GS}$  = -10V)  
 Max  $R_{DS(ON)}$  < 7.5m $\Omega$  ( $V_{GS}$  = -10V)  
 Max  $R_{DS(ON)}$  < 12m $\Omega$  ( $V_{GS}$  = -4V)  
 ESD Rating: 4KV HBM

**UIS Tested!**  
**Rg, Ciss, Coss, Crss Tested**



**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>AF</sup>	$I_D$	$T_A=25^\circ\text{C}$	-15
		$T_A=70^\circ\text{C}$	-13.6
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	-60	A
Avalanche Current <sup>G</sup>	$I_{AR}$	40	A
Repetitive avalanche energy L=0.3mH <sup>G</sup>	$E_{AR}$	240	mJ
Power Dissipation <sup>A</sup>	$P_D$	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	26	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	50	$^\circ\text{C/W}$
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	14	24	$^\circ\text{C/W}$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -10	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =-250μA	-0.9	-1.25	-1.6	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-60			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-15A T <sub>J</sub> =125°C		6.7 9.4	7.5 12	mΩ
		V <sub>GS</sub> =-4V, I <sub>D</sub> =-13A		9.2	12	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-15A		60		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.69	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				5.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz		5500	6600	pF
C <sub>OSS</sub>	Output Capacitance			745		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			473		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		3.1	4	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-15A		88.8	120	nC
Q <sub>g(4.5V)</sub>	Gate Charge			45.2	60	nC
Q <sub>gs</sub>	Gate Source Charge			10.1		nC
Q <sub>gd</sub>	Gate Drain Charge			19.4		nC
t <sub>D(on)</sub>	Turn-On DelayTime			12		ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =1.7Ω, R <sub>GEN</sub> =3Ω		11.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			100		ns
t <sub>f</sub>	Turn-Off Fall Time			40		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-15A, di/dt=100A/μs		46.6	60	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-15A, di/dt=100A/μs		67.7		nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using <300μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s thermal resistance rating.

G: EAR and IAR ratings are based on low frequency and duty cycles such that T<sub>J(start)</sub>=25C for each pulse.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

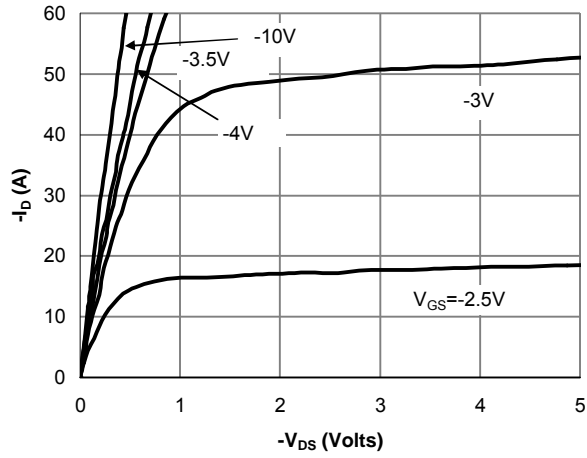


Fig 1: On-Region Characteristics

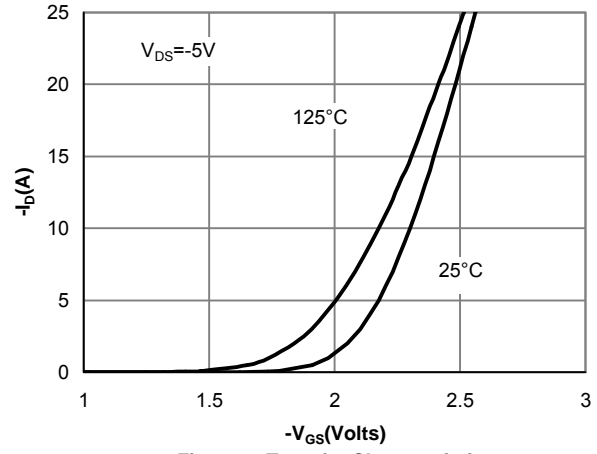


Figure 2: Transfer Characteristics

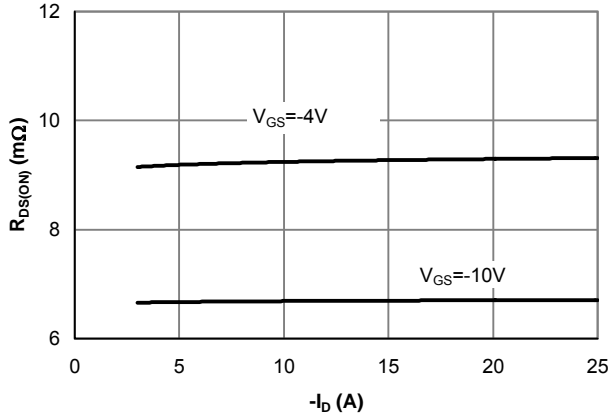


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

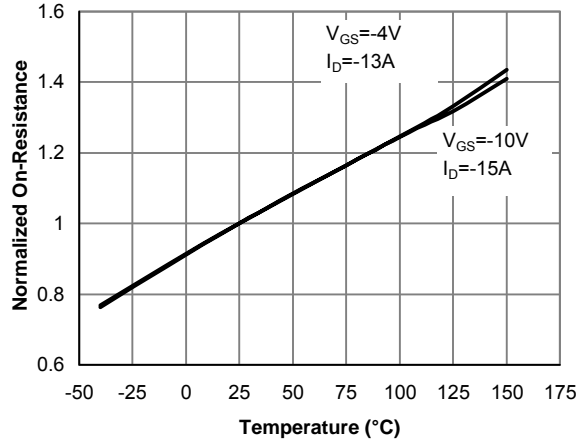


Figure 4: On-Resistance vs. Junction Temperature

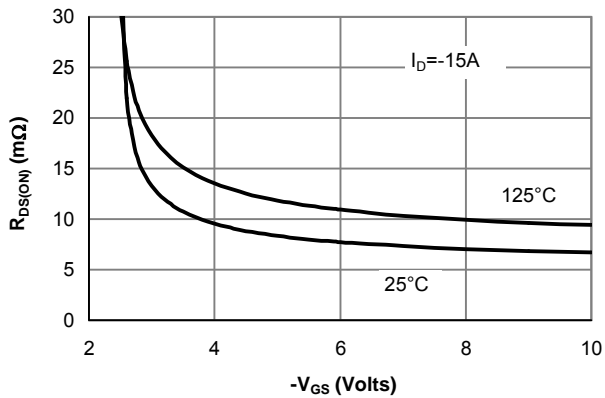


Figure 5: On-Resistance vs. Gate-Source Voltage

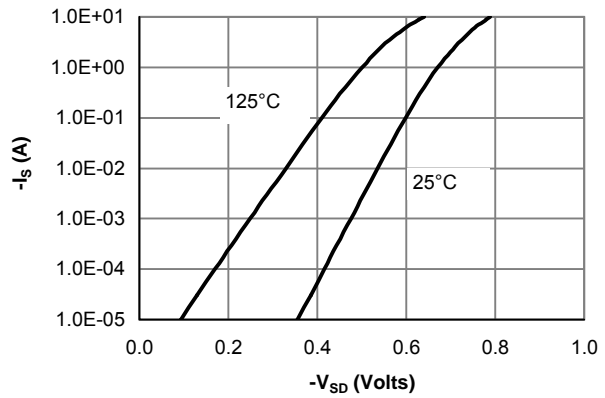


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

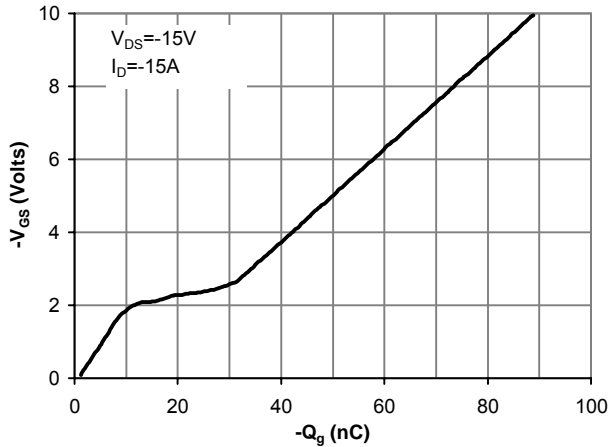


Figure 7: Gate-Charge Characteristics

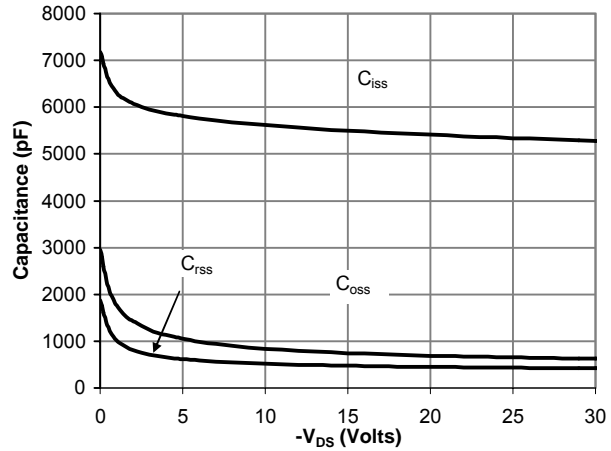


Figure 8: Capacitance Characteristics

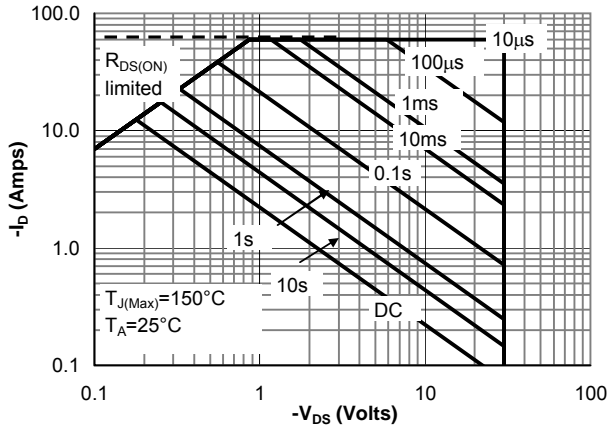


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

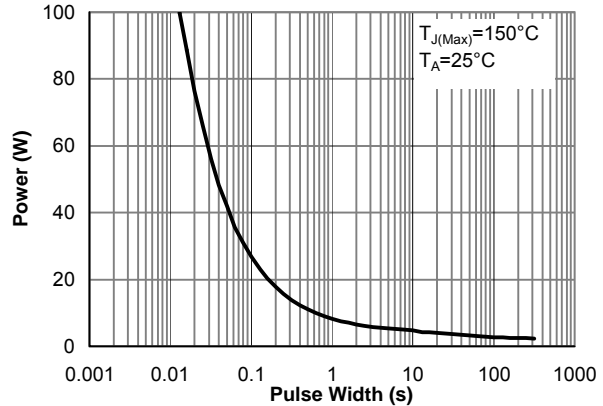


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

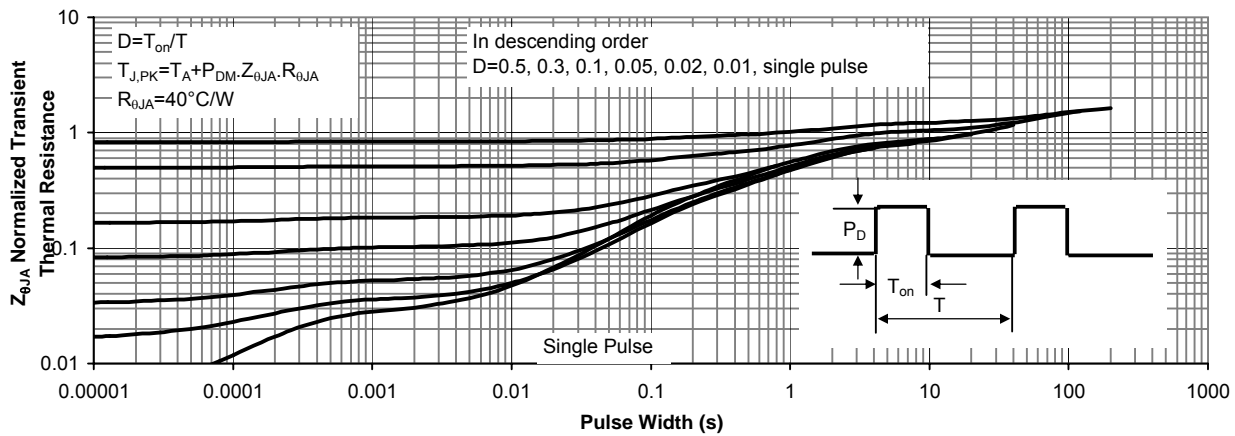


Figure 11: Normalized Maximum Transient Thermal Impedance