2N6379*

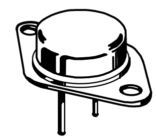
*Motorola Preferred Device

High-Power PNP Silicon Transistors

. . . designed for use in industrial–military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 120 Vdc (Min) — 2N6379
- High DC Current Gain —
  h_{FE} = 30 – 120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35µs (Max)
  t_s = 0.8 µs (Max)
  t_f = 0.25 µs (Max)
- Complement to 2N6274–77

**50 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
250 WATTS**



**CASE 197A–05
TO–204AE
(TO–3)**

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	140	Vdc
Collector–Emitter Voltage	V_{CEO}	120	Vdc
Emitter–Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous Peak	I_C	50 100	Adc
Base Current	I_B	20	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

* Indicates JEDEC Registered Data.

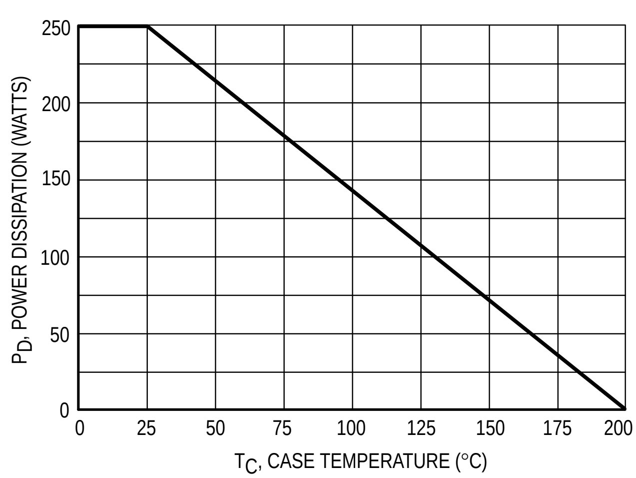


Figure 1. Power Derating

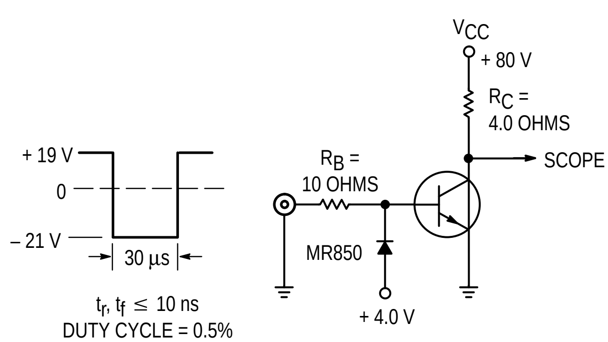
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector–Emitter Sustaining Voltage(1) (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	120	—	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, I_B = 0)	I_{CEO}	—	50	µAdc
Collector Cutoff Current (V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 10 1.0	 µAdc mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	100	µAdc
***ON CHARACTERISTICS(1)**				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 20 Adc, V_{CE} = 4.0 Vdc) (I_C = 50 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 50 30 10	 — 120 —	—
Collector–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 2.0 Adc) (I_C = 50 Adc, I_B = 10 Adc)	$V_{CE(sat)}$	— — —	 1.2 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 2.0 Adc) (I_C = 50 Adc, I_B = 10 Adc)	$V_{BE(sat)}$	 — —	 1.8 3.5	Vdc
DYNAMIC CHARACTERISTICS				
*Current–Gain — Bandwidth Product(2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	—	MHz
*Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	1500	pF
***SWITCHING CHARACTERISTICS (Figure 2)**				
Rise Time — (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_r	—	0.35	µs
Storage Time — (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_s	—	0.80	µs
Fall Time — (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_f	—	0.25	µs

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$



NOTE: For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

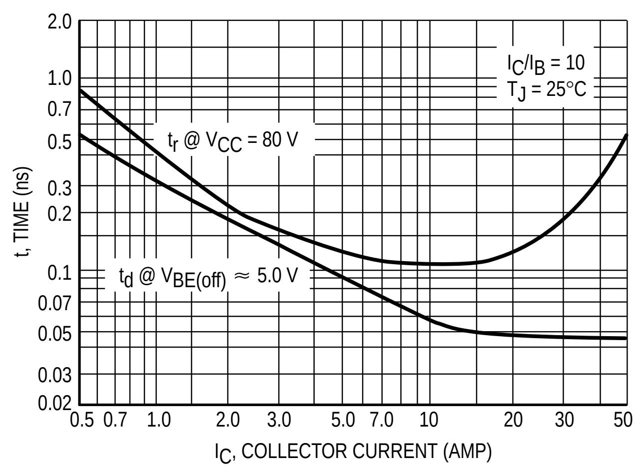


Figure 3. Turn–On Time

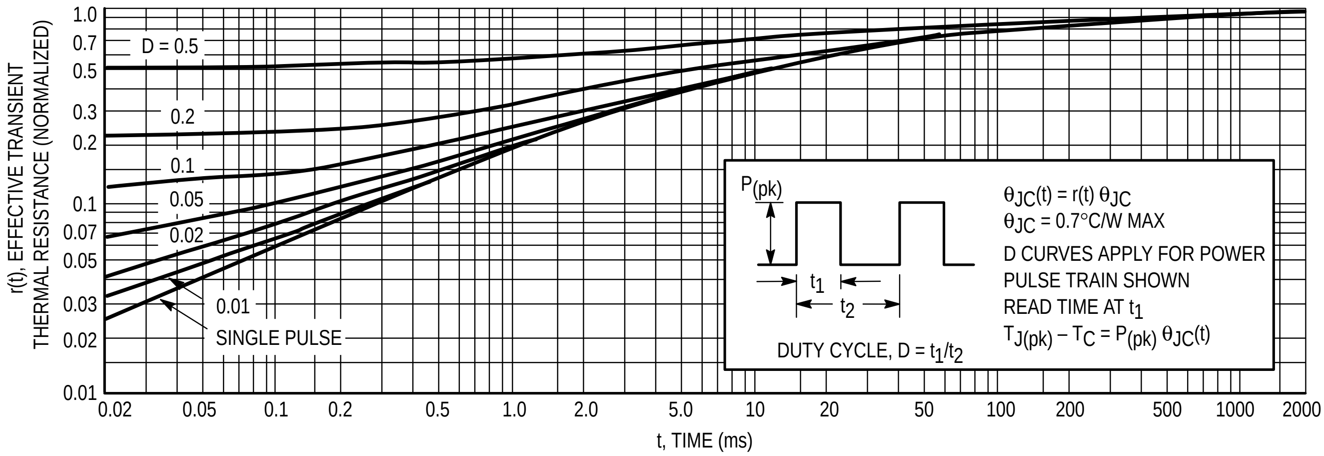


Figure 4. Thermal Response

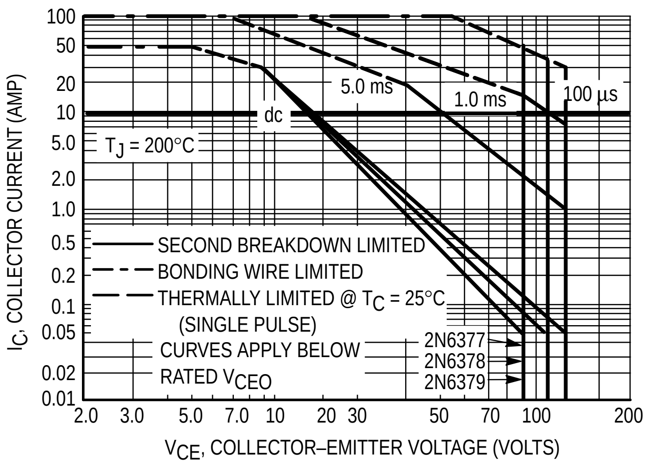


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

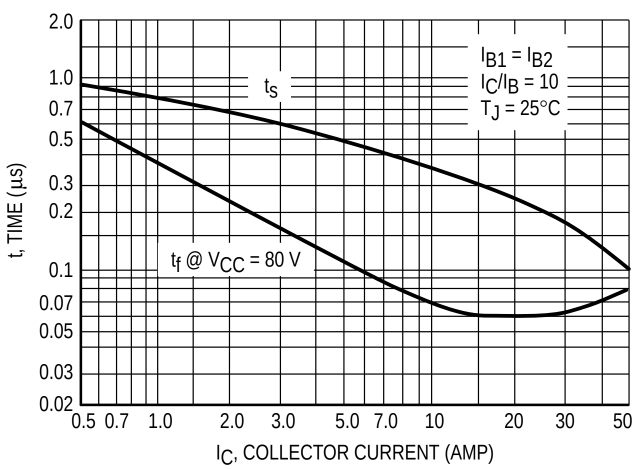


Figure 6. Turn–Off Time

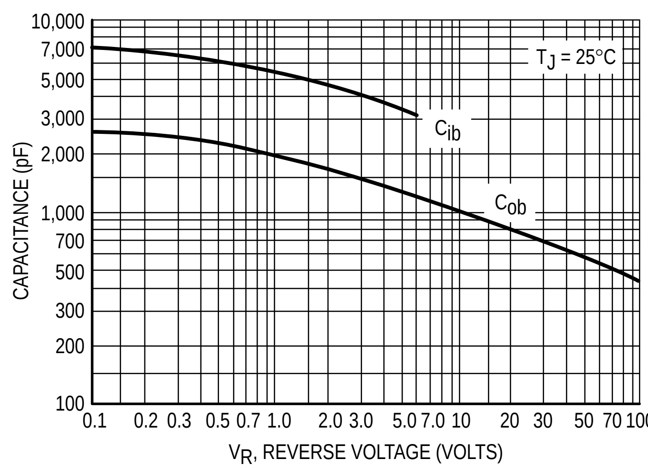


Figure 7. Capacitance

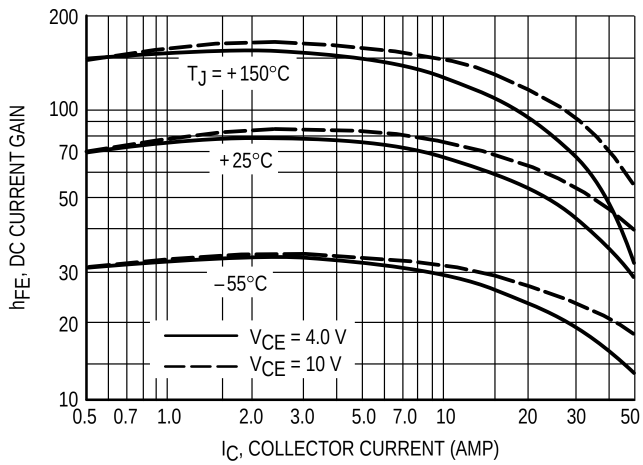


Figure 8. DC Current Gain

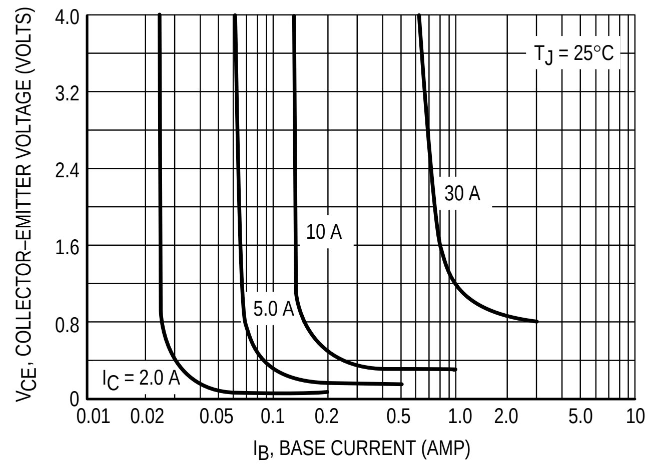


Figure 9. Collector Saturation Region

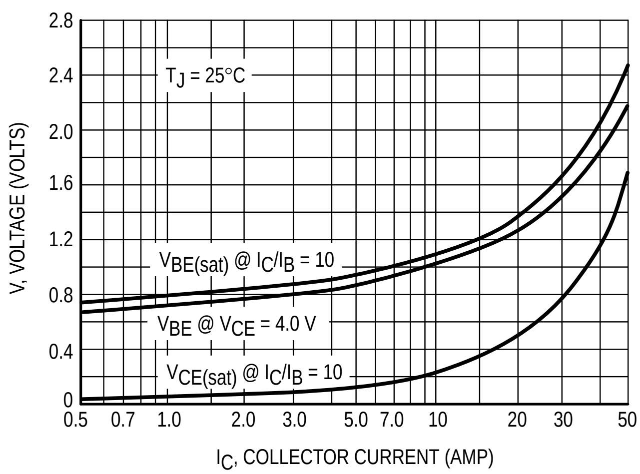


Figure 10. “On” Voltages

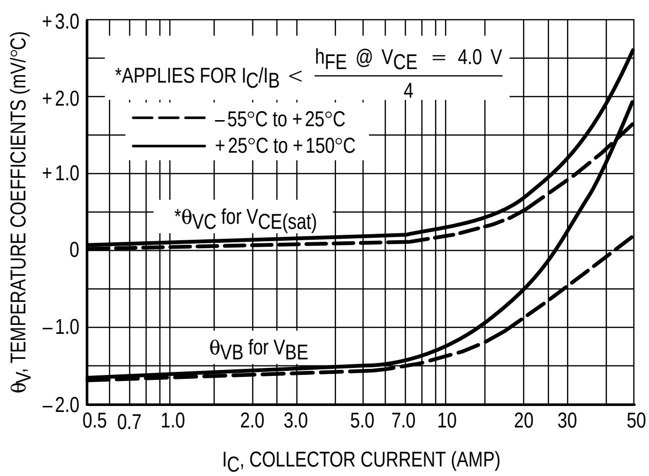


Figure 11. Temperature Coefficients

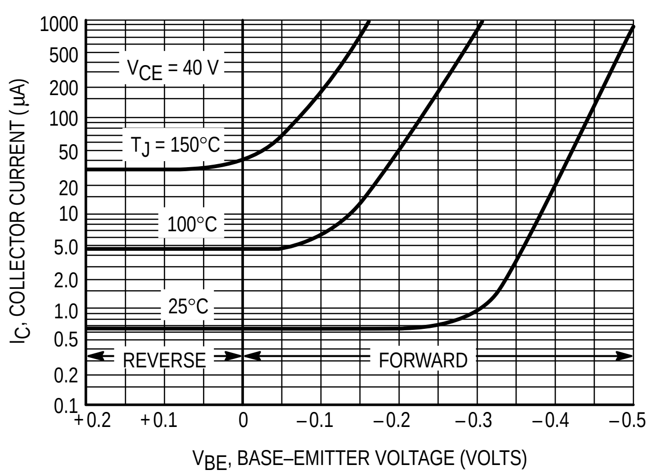


Figure 12. Collector Cut–Off Region

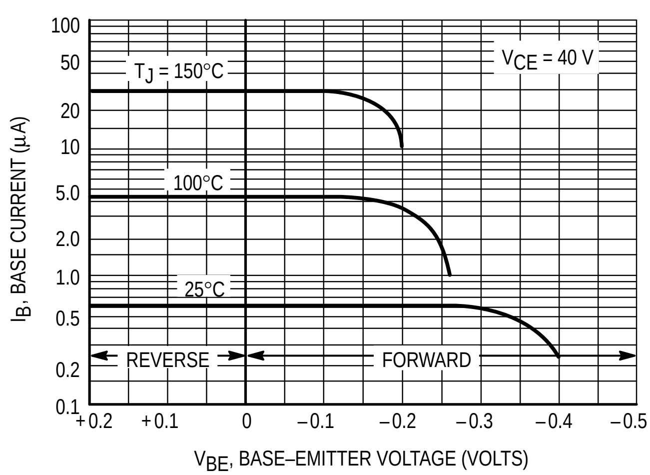
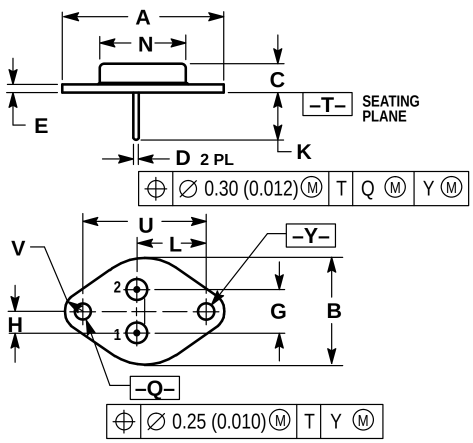


Figure 13. Base Cutoff Region

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 197A–05
TO–204AE (TO–3)
ISSUE J

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