

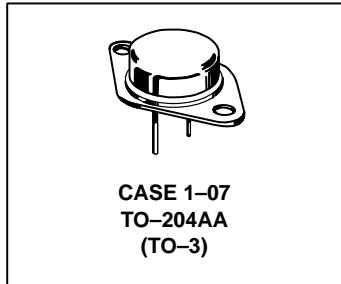
Complementary Silicon High-Power Transistors

... designed for general-purpose power amplifier and switching applications.

- Low Collector–Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 5.0 \text{ Adc}$
- Low Leakage Current —
 $I_{CEX} = 0.5 \text{ mAdc (Max) @ Rated Voltage}$
- Excellent DC Current Gain —
 $h_{FE} = 20 \text{ (Min) @ } I_C = 4.0 \text{ Adc}$
- High Current Gain — Bandwidth Product —
 $f_T = 4.0 \text{ MHz (Min) @ } I_C = 0.5 \text{ A}$

NPN
2N5877
2N5878

10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60–80 VOLTS
150 WATTS



MAXIMUM RATINGS (1)

Rating	Symbol	2N5877	2N5878	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 20		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150 0.857		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

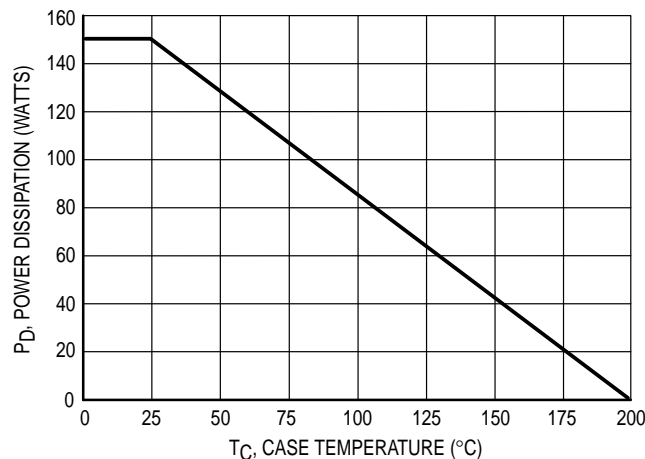


Figure 1. Power Derating

2N5877 2N5878

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mAdc}$, $I_B = 0$)	2N5877 2N5878	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	2N5877 2N5878	I_{CEO}	— —	1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	2N5877 2N5878 2N5877 2N5878	I_{CEX}	— — — —	0.5 0.5 5.0 5.0	mAdc
Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$)	2N5877 2N5878	I_{CBO}	— —	0.5 0.5	mAdc
Emitter Cutoff Current ($V_{EB} = 5.0 \text{ Vdc}$, $I_E = 0$)		I_{EBO}	—	1.0	mAdc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	35 20 4.0	— 100 —	—
Collector–Emitter Saturation Voltage (1) ($I_C = 5.0 \text{ Adc}$, $I_B = 0.5 \text{ Adc}$) ($I_C = 10 \text{ Adc}$, $I_B = 2.5 \text{ Adc}$)	$V_{CE(sat)}$	— —	1.0 3.0	Vdc
Base–Emitter Saturation Voltage (1) ($I_C = 10 \text{ Adc}$, $I_B = 2.5 \text{ Adc}$)	$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.5	Vdc

DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (2) ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 1.0 \text{ MHz}$)	f_T	4.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{ob}	—	300	pF
Small–Signal Current Gain ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	20	—	—

SWITCHING CHARACTERISTICS

Rise Time	($V_{CC} = 30 \text{ Vdc}$, $I_C = 4.0 \text{ Adc}$, $I_{B1} = I_{B2} = 0.4 \text{ Adc}$, See Figure 2)	t_r	—	0.7	μs
Storage Time		t_s	—	1.0	μs
Fall Time		t_f	—	0.8	μs

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{test}$.

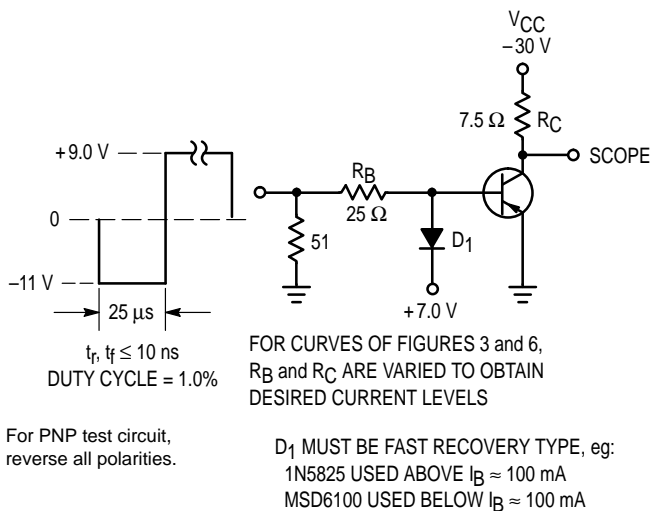


Figure 2. Switching Time Test Circuit

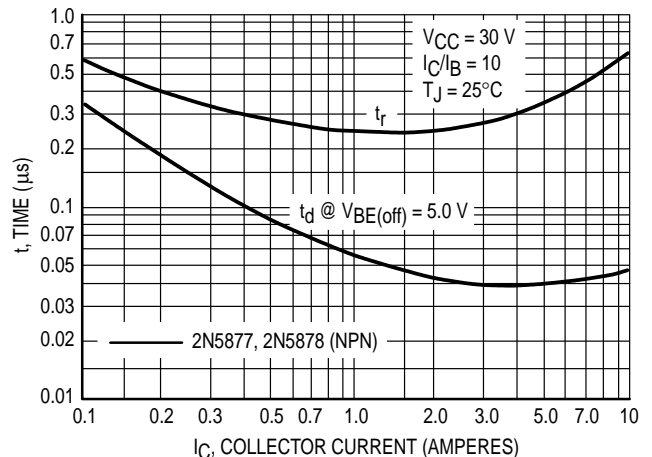


Figure 3. Turn–On Time

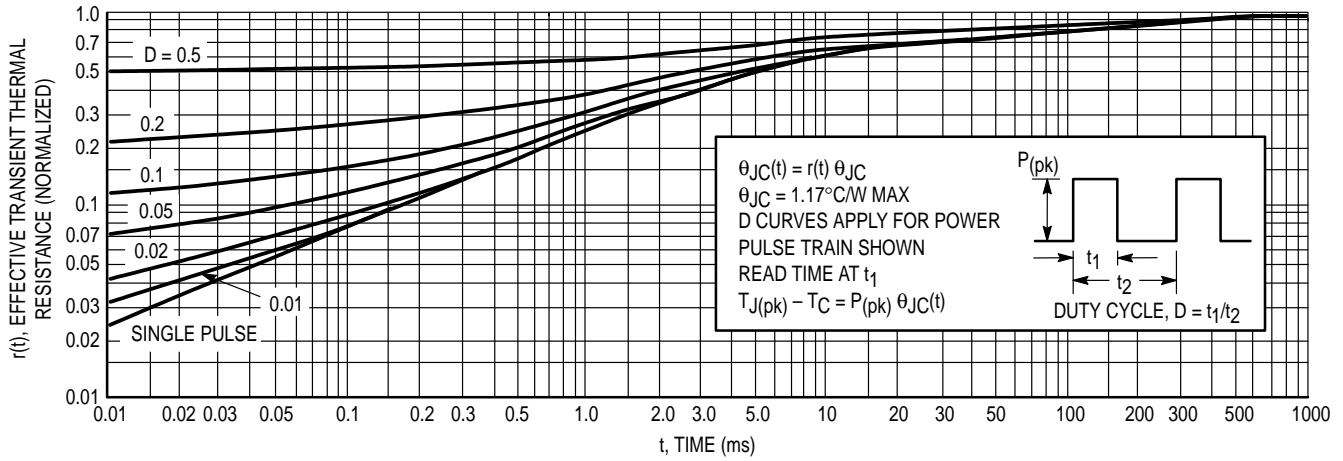


Figure 4. Thermal Response

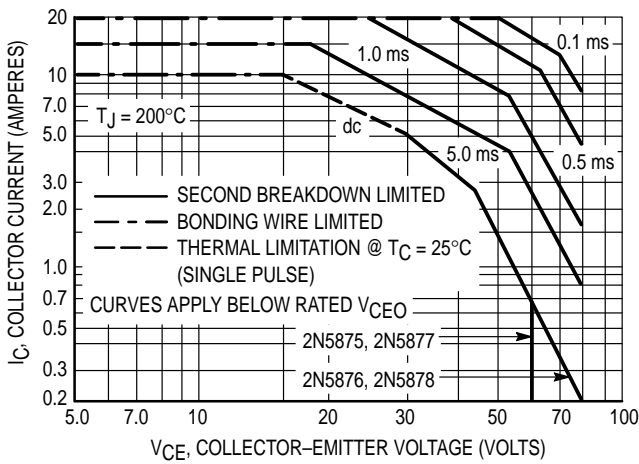


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_J(p_k) = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(p_k) < 200^\circ\text{C}$. $T_J(p_k)$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

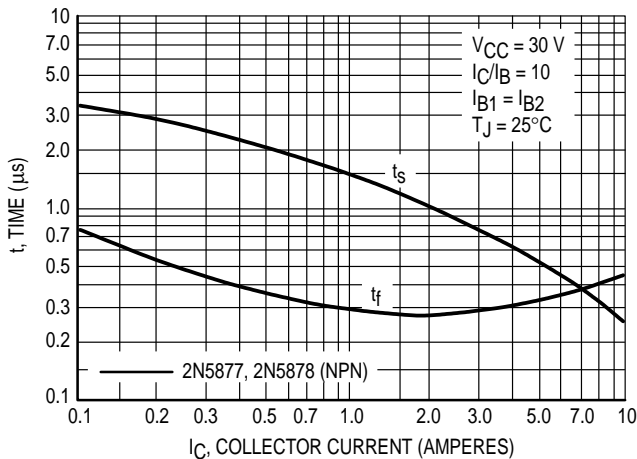


Figure 6. Turn-Off Time

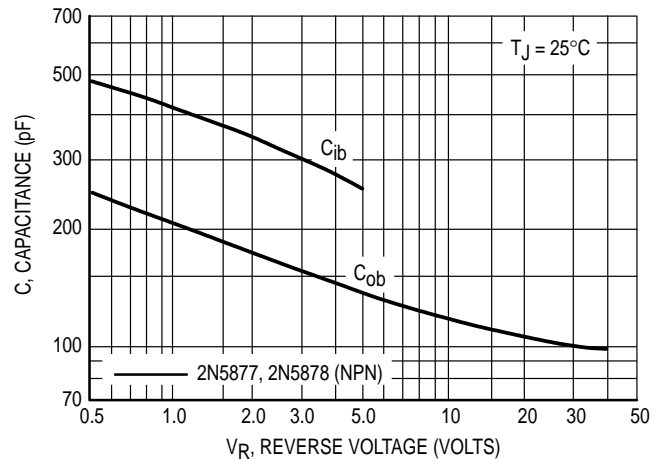
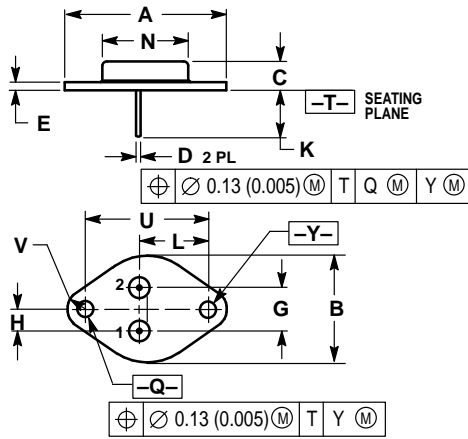


Figure 7. Capacitance

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

- STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

CASE 1-07
 TO-204AA (TO-3)
 ISSUE Z

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