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DIGITAL Semiconductor SA-1100 Microprocessor

Data Sheet

EC–R8XUA–TE

Revision/Update Information: This is a new document.

Digital Equipment Corporation
Maynard, Massachusetts

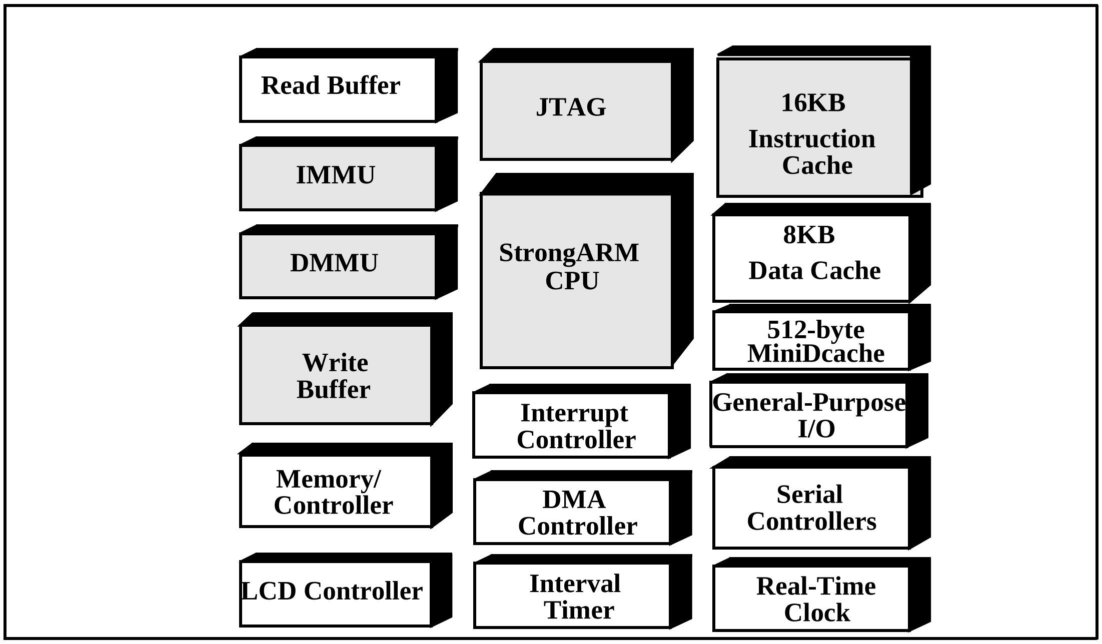
http://www.digital.com/semiconductor

January 1998

SA-1100 Microprocessor

The DIGITAL Semiconductor SA-1100 Microprocessor (SA-1100) is the second member of the StrongARM family. It is a highly integrated communications microcontroller that incorporates a 32-bit StrongARM RISC processor core, system support logic, multiple communication channels, an LCD controller, a PCMCIA controller, and general-purpose I/O ports.

As does the DIGITAL Semiconductor SA-110 Microprocessor (SA-110), the SA-1100 provides superior power efficiency, low cost, and the highest performance in the industry. The following diagram shows the features of the SA-1100. The shaded boxes are features that have carried over with few or no changes from the SA-110. The nonshaded boxes are new or updated features for the SA-1100.



Features of the SA-1100 CPU for AA and BA Parts

The SA-1100 CPU contains the following features:

- High performance
  - → 150 Dhrystone 2.1 MIPS @ 133 MHz
  - → 230 Dhrystone 2.1 MIPS @ 200 MHz
- Low power (normal mode) *
  - → <200 mW @ 1.5 V/133 MHz
  - → <250 mW @ 1.5 V/200 MHz
- Integrated clock generation
  - → Internal phase-locked loop (PLL)
  - → 3.686-MHz oscillator
  - → 32.768-kHz oscillator
- Power-management features
  - → Normal (full-on) mode
  - → Idle (power-down) mode
  - → Sleep (power-down) mode
- Big and little endian operating modes
- 3.3-V I/O interface
- 208-pin thin quad flat pack (LQFP)**
- 32-way set-associative caches
  - → 16KB instruction cache
  - → 8KB write-back data cache
- 32-entry memory-management units
  - → Maps 4KB, 8KB, or 1MB
- Write buffer
  - → 8-entry, between 1 and 16 bytes each
- Read buffer
  - → 4-entry, 1, 4, or 8 words
- Memory bus
  - → Interfaces to ROM, Flash, SRAM, and DRAM
  - → Supports two PCMCIA sockets

* Power dissipation, particularly in idle mode, is strongly dependent on the details of the system design.

** DIGITAL Semiconductor has modified its package nomenclature due to industry standardization of packages. LQFP is 1.4mm thick, thin quad flat pack. Please note that *no* modification has been made to the package itself.

SA-1100 Microprocessor

Features of the SA-1100 CPU for CA and DA Parts

The SA-1100 CPU contains the following features:

- High performance
  - → 180 Dhrystone 2.1 MIPS @ 160 MHz
  - → 250 Dhrystone 2.1 MIPS @ 220 MHz
- Low power (normal mode) *
  - → <320 mW @ 2.0 V/160 MHz
  - → <450 mW @ 2.0 V/220 MHz
- Integrated clock generation
  - → Internal phase-locked loop (PLL)
  - → 3.686-MHz oscillator
  - → 32.768-kHz oscillator
- Big and little endian operating modes
- 3.3-V I/O interface
- 208-pin thin quad flat pack (LQFP)**
- 32-way set-associative caches
  - → 16KB instruction cache
  - → 8KB write-back data cache
- 32-entry memory-management units
  - → Maps 4KB, 8KB, or 1MB
- Write buffer
  - → 8-entry, between 1 and 16 bytes each
- Read buffer
  - → 4-entry, 1, 4, or 8 words
- Memory bus
  - → Interfaces to ROM, Flash, SRAM, and DRAM
  - → Supports two PCMCIA sockets

* Power dissipation, particularly in idle mode, is strongly dependent on the details of the system design.

** DIGITAL Semiconductor has modified its package nomenclature due to industry standardization of packages. LQFP is 1.4mm thick, thin quad flat pack. Please note that *no* modification has been made to the package itself.

Changes to the SA-110 Core

The SA-110 core has the following changes:

- Data cache reduced from 16KB to 8KB
- Interrupt vector address adjust capability
- Read buffer (nonblocking)
- Minicache for alternate data caching
- Hardware breakpoints
- Memory-management unit (MMU) enhancements
- Process ID mapping

Additional Features Built into SA-1100 Chipset

Features added to the SA-1100 chipset include:

- Memory controller supporting ROM, Flash, EDO, standard DRAM, and SRAM
- LCD controller
  - → 1-, 2-, or 4-bit gray-scale levels
  - → 8-, 12-, or 16-bit color levels
- Serial communications module supporting SDLC
- 230-Kb/s UART
- Touch-screen, audio, telecom port
- IrDA serial port
  - → 115 Kb/s, 4 Mb/s
- Six-channel DMA controller
- Integrated two-slot PCMCIA controller
- Twenty-eight general-purpose I/O ports
- Real-time clock with interrupt capability
- Onchip oscillators for clock sources
- Interrupt controller
- Power-management features
  - → Normal (full-on) mode
  - → Idle (power-down) mode
  - → Sleep (power-down) mode
- Four general-purpose interruptible timers
- 12-Mb/s USB device controller
- Synchronous serial port (UCB1100, UCB1200, SPI, TI, µWire)

Applications for AA and BA Parts

- Handheld personal computers
- Smart phones
- Digital cameras
- Subnotebooks
- Wallet personal computers
- Portable network computers

Applications for CA and DA Parts

- Screen/web phones
- Point-of-sale terminals
- POTS video phones
- Video kiosks
- Intelligent vending machines
- LCD-based network computers
- Modem controllers in modem banks

Operating Systems

- Apple – Newton OS
- JMI – C EXECUTIVE
- Lucent – Inferno
- Microsoft – Windows CE
- Microware – OS-9
- Psion – EPOC32
- Sun Microsystems – JavaOS
- Wind River – VxWorks

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1.0 Introduction

The DIGITAL Semiconductor SA-1100 Microprocessor (SA-1100) is a general-purpose, 32-bit RISC microprocessor with a 16KB instruction cache, an 8KB write-back data cache, a minicache, a write buffer, a read buffer, and a memory-management unit (MMU) combined in a single chip. The SA-1100 is software compatible with the ARM V4 architecture processor family and can be used with ARM support chips such as I/O, memory, and video. The core of the SA-1100 is derived from the core of the DIGITAL Semiconductor SA-110 Microprocessor (SA-110), with the following changes:

- Reduction in size of the data cache from 16KB to 8KB
- Addition of a 512-byte mini data cache that allocates based on MMU settings
- Addition of debug support in the form of address and data breakpoints
- Addition of a four-entry read buffer to facilitate software-controlled data prefetching
- Addition of vector address adjust capability
- Addition of a process ID register

The logic outside the core and caches is grouped into the following three modules:

- Memory and PCMCIA control module (MPCM)
  - Memory interface supporting ROM, Flash, DRAM, SRAM and PCMCIA control signals
- System control module (SCM)
  - Twenty-eight general-purpose interruptible I/O ports
  - Real-time clock, watchdog, and interval timers
  - Power management controller
  - Interrupt controller
  - Reset controller
  - Two onchip oscillators for connection to 3.686-MHz and 32.768-kHz crystals
- Peripheral control module (PCM)
  - Six-channel DMA controller
  - Gray/color, active/passive LCD controller
  - 230-Kb/s SDLC controller
  - 16550-compatible UART
  - IrDA serial port (115 Kb/s, 4 Mb/s)
  - Synchronous serial port (UCB1100, UCB1200, SPI, TI, µWire)
  - Universal serial bus (USB) device controller

The instruction set comprises eight basic instruction types:

- Two of these types make use of the onchip arithmetic logic unit, barrel shifter, and multiplier to perform high-speed operations on the data in a bank of 16 logical registers (31 physical registers), each 32 bits wide.
- Three classes of instructions control data transfer between memory and the registers: one optimized for flexibility of addressing, one for rapid context switching, and one for swapping data.
- Two instructions control the flow and privilege level of execution.
- One class is used to access the privileged state of the CPU.

The ARM instruction set is a good target for compilers of many different high-level languages. Where required for critical code segments, assembly code programming is also straightforward, unlike some RISC processors that depend on sophisticated compiler technology to manage complicated instruction interdependencies.

The SA-1100 is a static part and has been designed to run at a reduced voltage to minimize its power requirements. This makes it ideal for portable applications where both of these features are essential.

1.1 Example System

Figure 1 shows how the SA-1100 can be used in a handheld computing device.

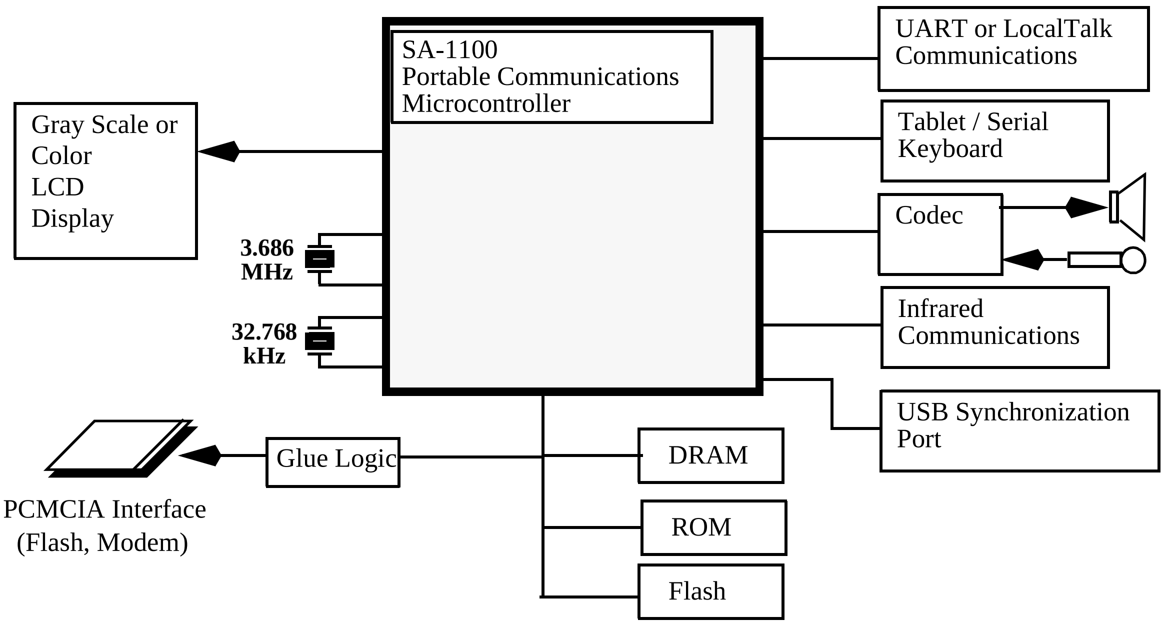

Figure 1 SA-1100 Example System

1.2 ARM Architecture

The SA-1100 implements the ARM V4 architecture as defined in the *ARM Architecture Reference*, 28-July-1995, with the following options:

1.2.1 26-Bit Mode

The SA-1100 supports 26-bit mode but all exceptions are initiated in 32-bit mode. The P and D bits do not affect the operation of SA-1100; they are always read as ones and writes to them are ignored.

1.2.2 Coprocessors

The SA-1100 supports MCR and MRC access to coprocessor number 15. These instructions are used to access the memory-management, configuration, and cache control registers. In addition, coprocessor 15 provides control for read buffer fills and flushes, and hardware breakpoints. All other coprocessor instructions cause an undefined instruction exception. No support for external coprocessors is provided.

1.2.3 Memory Management

Memory management exceptions preserve the base address registers so that no code is required to restore state. Separate translation lookaside buffers (TLBs) are implemented for the instruction and data streams. Each TLB has 32 entries that can each map a segment, a large page, or a small page. The TLB replacement algorithm is round robin. The data TLBs support both the flush-all and flush-single-entry operations, while the instruction TLBs support only the flush-all operation.

1.2.4 Instruction Cache

The SA-1100 has a 16KB instruction cache (Icache) with 32-byte blocks and 32-way associativity. The cache supports the flush-all function. Replacement is round robin within a set. The Icache can be enabled while memory management is disabled. When memory management is disabled, all memory is considered cacheable by the Icache.

1.2.5 Data Cache

The SA-1100 has an 8KB data cache (Dcache) with 32-byte blocks and 32-way associativity. The cache supports the flush-all, flush-entry, and copyback-entry functions. The copyback-all function is not supported in hardware. This function can be provided by software. The cache is read allocate with round-robin replacement.

The Dcache has been augmented with a 16-entry, two-way set associative minicache that allocates when the MMU **b** and **c** bits are 0 and 1, respectively. This cache is accessed in parallel with the main Dcache. Replacement victims in this cache are replaced based on a least-recently-used (LRU) algorithm. This cache is useful for applications that access large data structures and would normally thrash the main Dcache. Instead, these data structures can be mapped so that they allocate into the minicache and only replace data from the same structure.

1.2.6 Write Buffer

The SA-1100 has an eight-entry write buffer with each entry able to contain 1 to 16 bytes. A drain write buffer operation is supported.

1.2.7 Read Buffer

The SA-1100 has a four-entry read buffer capable of loading 1, 4, or 8 words of data per entry. This facility permits software to preload data into the buffer for use at a later time without blocking the operation of the processor. Software can flush either a single entry or the entire buffer (four entries). The read buffer is controlled through system control coprocessor 15 and can be enabled for use in user mode.

2.0 SA-1100 Functional Description

This chapter provides a functional description of the SA-1100 integrated processor. It describes the basic building blocks within the chip, lists and describes the pins, and explains the memory map.

2.1 Block Diagram

The SA-1100 consists of the following functional blocks:

- **Processor**
  The processor is the StrongARM SA-1 core with a 16KB instruction and 8KB Dcache. The I and D streams are translated through independent memory-management units (MMUs). Stores are made using a four-line write buffer. The performance of specialized load routines is enhanced with the four-entry read buffer that can be used to prefetch data for use at a later time. A 16-entry minicache provides a smaller and logically separate data cache that can be used to enhance caching performance when dealing with large data structures.
- **Memory and PCMCIA controller**
  The memory and PCMCIA control module (MPCM) supports four banks of standard or EDO DRAM on a 32-bit data width. ROM (standard and burst), Flash memory, and SRAM are also supported. ROM and Flash can be either 16 or 32 bits wide. SRAM width is limited to 32 bits. Expansion devices are supported through PCMCIA control signals that share the memory bus data and address lines to complete the card interface. Some external glue logic (buffers and transceivers) is necessary to implement the interface. Control is provided to permit two card slots with hot-swap capability.
- **Peripherals**
  The peripheral control module (PCM) contains a number of serial control devices, an LCD controller as well as a six-channel DMA controller to provide service to these devices:
  – An LCD controller with support for passive or active displays
  – A universal serial bus (USB) endpoint controller
  – An SDLC communications controller
  – A serial controller with supporting 115-Kb/s and 4-Mb/s IrDA protocols
  – A 16550-like UART supporting 230 Kb/s
  – A CODEC interface supporting SPI, µWire, TI, UCB1100, and UCB1200
- **General system control functions**
  The system control module (SCM) is also connected to the peripheral bus. It contains five blocks used for general system functions:
  – A real-time clock (RTC) clocked from an independent 32.768-kHz oscillator
  – An operating system timer (OST) for general system timer functions as well as a watchdog mode
  – Twenty-eight general-purpose I/Os (GPIO)
  – An interrupt controller
  – A power-management controller that handles the transitions in and out of sleep and idle modes
  – A reset controller that handles the various reset sources on the chip

Figure 2 shows the functional blocks contained in the SA-1100 integrated processor. Figure 3 is a functional diagram of the SA-1100.

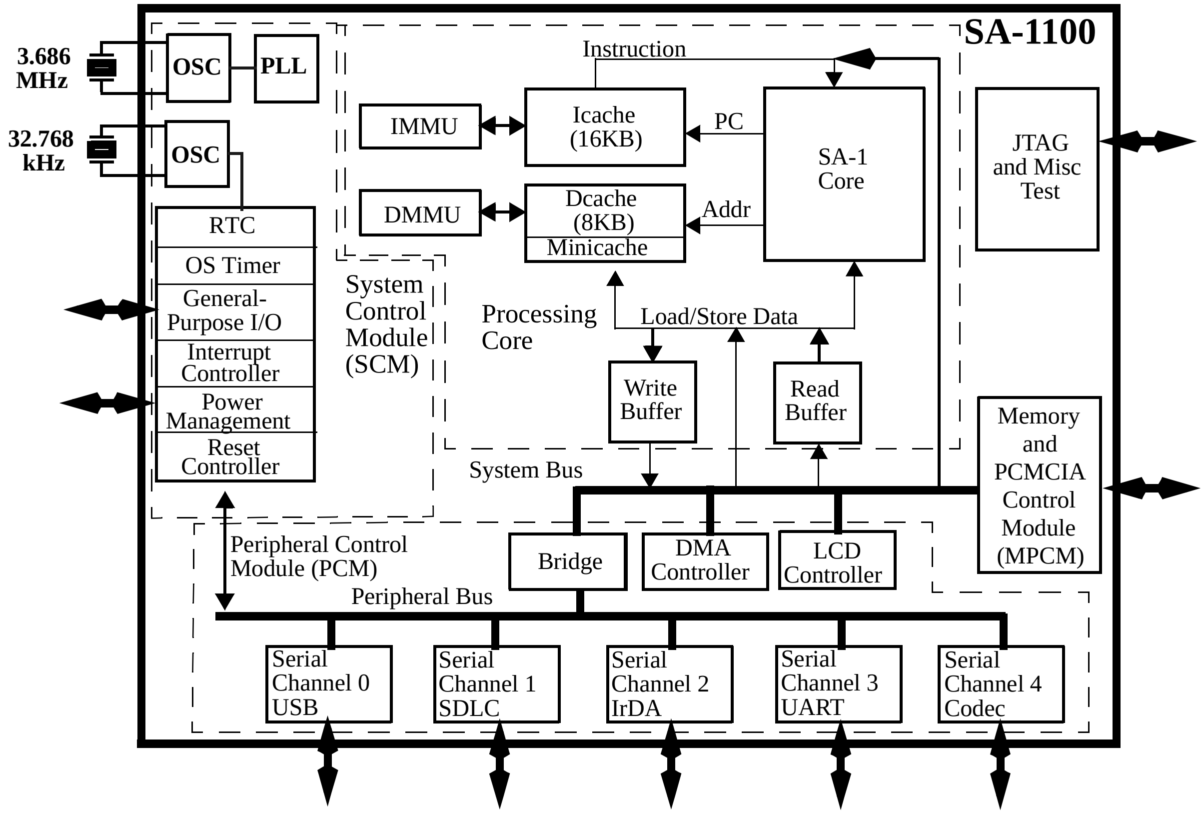

Figure 2 SA-1100 Block Diagram

2.2 Inputs/Outputs

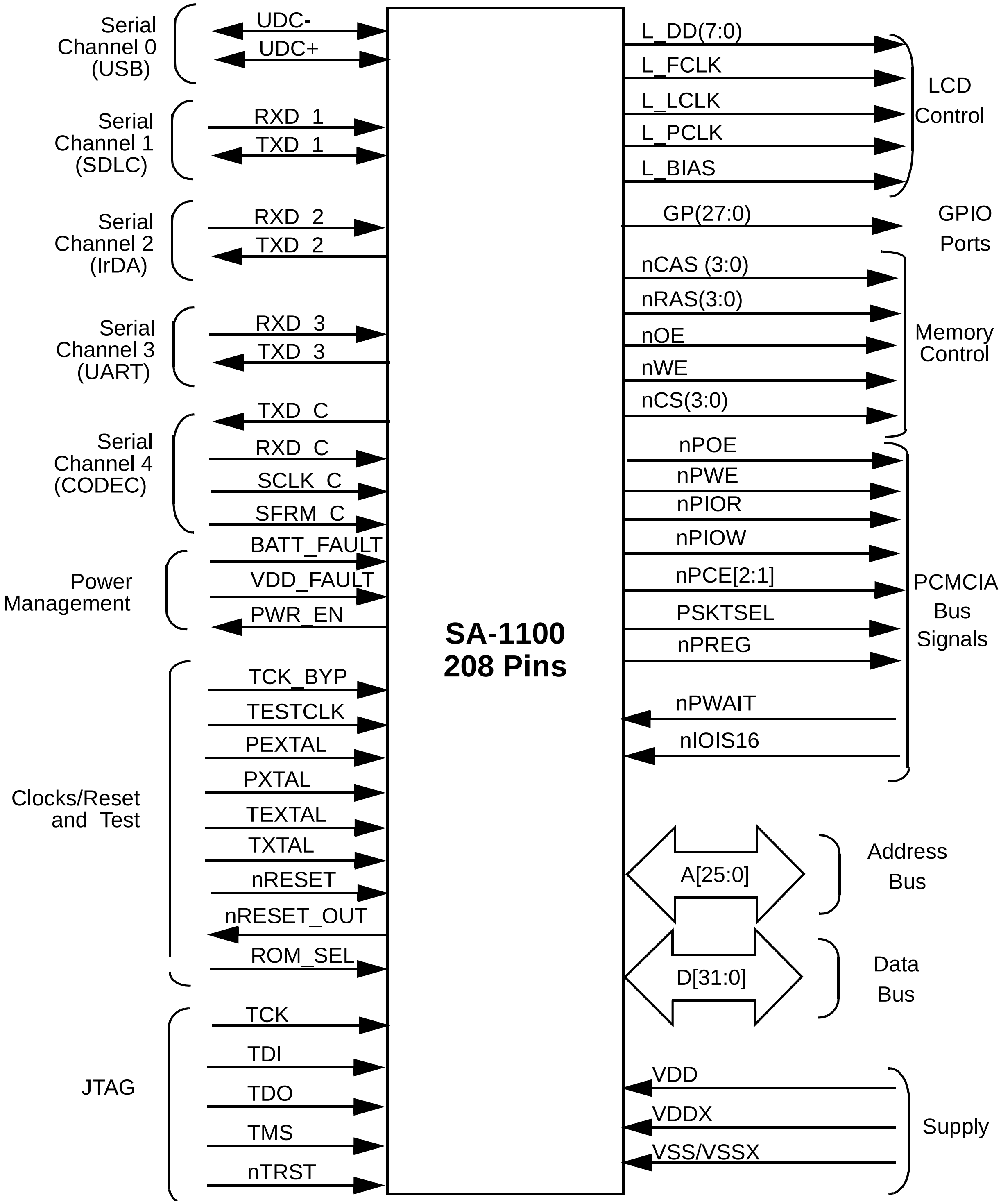

Figure 3 SA-1100 Functional Diagram

2.3 Signal Description

The following table describes the signals.

Key to Signal Types:
n – Active low signal
IC – Input, CMOS threshold
ICOCZ – Input, CMOS threshold, output CMOS levels, tristatable
OCZ – Output, CMOS levels, tristatable

Name	Type	Description
A[25:0]	OCZ	Memory address bus. This bus signals the address requested for memory accesses. Bits 21..10 carry the 12-bit DRAM address, the static memory devices, and the expansion bus receive address bits 25..0.
D[31:0]	ICOCZ	Memory data bus.
nCS[3:0]	OCZ	Static chip selects. These signals are chip selects to static memory devices such as ROM and Flash. They are individually programmable in the memory configuration registers.
nOE	OCZ	Memory output enable. This signal should be connected to the output enables to begin driving data onto the data bus.
nWE	OCZ	DRAM write enable. This signal should be connected to the DRAM write enables to perform writes. This signal is used in conjunction with **CAS[3:0]** to perform byte writes.
nRAS[3:0]	OCZ	DRAM RAS. These signals should be connected to the DRAM row address strobe (RAS) pin.
nCAS[3:0]	OCZ	DRAM CAS. These signals should be connected to the DRAM column address strobe (CAS) pins.
nPOE	OCZ	PCMCIA output enable. This PCMCIA signal is an output and is used to perform reads from memory and attribute space.
nPWE	OCZ	PCMCIA write enable. This signal is an output and is used to perform writes to memory and attribute space.
nPIOW	OCZ	PCMCIA I/O write. This signal is an output and is used to perform write transactions to the PCMCIA I/O space.
nPIOR	OCZ	PCMCIA I/O read. This signal is an output and is used to perform read transactions from the PCMCIA I/O space.
nPCE[2:1]	OCZ	PCMCIA card enable. These signals are output and are used to select a PCMCIA card. Bit one enables the high-byte lane and bit zero enables the low-byte lane.
nIOIS16	IC	I/O Select 16. This signal is an input and is an acknowledgement from the PCMCIA card that the current address is a valid 16-bit wide I/O address.
nPWAIT	IC	PCMCIA wait. This signal is an input and is driven low by the PCMCIA card to extend the length of the transfers to/from the SA-1100.
PSKTSEL	OCZ	PCMCIA socket select. This signal is an output and is used by external steering logic to route control, address, and data signals to one of the PCMCIA sockets. When **PSKTSEL** is low, socket zero is selected. When **PSKTSEL** is high, socket one is selected. This signal has the same timing as the address lines.
nPREG	OCZ	PCMCIA register select. This signal is an output and indicates that, on a memory transaction, the target address is attribute space. This signal has the same timing as address.

Name	Type	Description
L_DD[7:0]	OCZ	LCD controller display data.
L_FCLK	OCZ	LCD frame clock.
L_LCLK	OCZ	LCD line clock.
L_PCLK	OCZ	LCD pixel clock.
L_BIAS	OCZ	LCD ac bias drive.
TXD_C	OCZ	CODEC transmit.
RXD_C	IC	CODEC receive.
SCLK_C	OCZ	CODEC clock.
SFRM_C	OCZ	CODEC frame signal.
UDC+	OCZ	Serial port zero transmit pin (UDC).
UDC-	IC	Serial port zero receive pin (UDC).
TXD_1	OCZ	Serial port one transmit pin (SDLC).
RXD_1	IC	Serial port one receive pin (SDLC).
TXD_2	OCZ	Serial port two transmit pin (IrDA).
RXD_2	IC	Serial port two receive pin (IrDA).
TXD_3	OCZ	Serial port three transmit pin (UART).
RXD_3	IC	Serial port three receive pin (UART).
GP[27:0]	ICOCZ	General-purpose input output.
ROM_SEL	IC	ROM select. This pin is used to configure the ROM width. It is either grounded or pulled high. If **ROM_SEL** is grounded, the ROM width is 16 bits. If **ROM_SEL** is pulled up, the ROM width is 32 bits.
PXTAL	IC	Input connection for 3.686-MHz crystal.
PEXTAL	OCZ	Output connection for 3.686-MHz crystal.
TXTAL	IC	Input connection for 32.768-kHz crystal.
TEXTAL	OCZ	Output connection for 32.768-kHz crystal.
PWR_EN	OCZ	Power enable. Active high. **PWR_EN** enables the external power supply. Negating it signals the power supply that the system is going into sleep mode and that the **VDD** power supply should be removed.
BATT_FAULT	IC	Battery fault. Signals the SA-1100 that the main power source is going away (battery is low or has been removed from the system). The assertion of **BATT_FAULT** causes the SA-1100 to enter sleep mode. The SA-1100 will not recognize a wake-up event while this signal is asserted.
VDD_FAULT	IC	VDD fault. Signals the SA-1100 that the main power supply is going out of regulation (shorted card is inserted). **VDD_FAULT** will cause the SA-1100 to enter sleep mode. **VDD_FAULT** is ignored after a wake-up event until the poser supply timer completes (approximately 10 ms).

Name	Type	Description
nRESET	IC	Hard reset. This active low signal is a level-sensitive input used to start the processor from a known address. A low level will cause the current instruction to terminate abnormally, and the onchip caches, MMU, and write buffer to be disabled. When **nRESET** is driven high, the processor will restart from address 0. **nRESET** must remain low until the power supply is stable and the internal 3.686-MHz oscillator has come up to speed. While **nRESET** is low, the processor will perform idle cycles.
nRESET_OUT	OCZ	Reset out. This signal is asserted when **nRESET** is asserted and deasserts when the processor has completed resetting. **nRESET_OUT** is also asserted for "soft" reset events (sleep and watch-dog).
nTRST	IC	Test interface reset. Note this pin has an internal pull-down resistor and must be driven high to enable the JTAG circuitry. If left unconnected, this pin is pulled low and disables JTAG operation.
TDI	IC	JTAG test interface data input. Note this pin has an internal pull-up resistor.
TDO	OCZ	JTAG test interface data output. Note this pin does *not* have an internal pull-up resistor.
TMS	IC	JTAG test interface mode select. Note this pin has an internal pull-up resistor.
TCK	IC	JTAG test interface reference clock. This times all the transfers on the JTAG test interface. Note this pin has an internal pull-down resistor.
TCK_BYP	IC	Test clock PLL bypass. When **TCK_BYP** is high, the **TESTCLK** is used as the core clock in place of the PLL clock; when low, the internal PLL output is used. This signal has no relation to the JTAG **TCK** pin.
TESTCLK	IC	Test clock. **TESTCLK** is used to provide the core clock when **TCK_BYP** is high. It should be tied low if **TCK_BYP** is low. This pin should be used for test purposes only. An end user should ground this pin.
VDD	—	Positive supply for the core. Nine pins are allocated to this supply; eight pins are labeled **VDD**. The ninth pin, labeled **VDDP** is dedicated to the PLL supply and should be tied directly to the **VDD** power plane with the other eight **VDD** pins.
VDDX	—	Positive supply for the pins. Twenty pins are allocated to **VDDX**, labeled **VDDX1**, **VDDX2** and **VDDX3**. All of these pins should be tied directly to the **VDDX** power plane.
VSS	—	Ground supply. Nine pins are allocated to **VSS**, including one for the PLL.
VSSX	—	Ground supply for the I/O pins. Eighteen pins are allocated to **VSSX**.

2.4 Memory Map

Figure 4 shows the SA-1100 memory map. The map is divided into four main partitions of 1GB each.

The bottom partition is dedicated to static memory devices (ROM, SRAM, and Flash) and to the PCMCIA expansion bus area. It occupies addresses 0h0000 0000 through 0h3FFF FFFF. This space is divided into four 128MB blocks for static memory devices and two 256MB blocks for PCMCIA.

The static memory space is intended for ROM, SRAM, and Flash memory. The bottom partition (at 0h0000 0000) is assumed to be ROM at boot time. The width of the boot ROM is determined by the state of the **ROMSEL** pin. The PCMCIA interface is divided into Socket 0 and Socket 1 space. These partitions are further subdivided into I/O, memory and attribute space.

The next partition (0h4000 0000 to 0h7FFF FFFF) is reserved. Accessing this reserved space results in a data abort exception.

The third partition (0h8000 0000 to 0hBFFF FFFF) contains all onchip registers (except those specified by the ARM V4 architecture). This block is further subdivided into four blocks of 256MB each. They contain control registers for the major functional blocks within the chip (MECM, SCM, PCM). The LCD and DMA controllers are separate from the rest of the PCM and occupy the top 256MB partition.

The fourth partition (0hC000 0000 to 0hFFFF FFFF) contains DRAM memory. The bank sizes for DRAM are fixed at 128MB each. With multiple banks implemented, there probably will be gaps in the map that should be mapped through the memory-management unit. The next 128MB block in this partition is mapped within the memory controller and returns zeros when read. This function is intended to facilitate rapid cache flushing by not requiring an external memory access to load data into the cache. This space is burstable. Writes to this space have no effect. The top 384MB of this partition is reserved. Accessing this space causes a data abort exception.

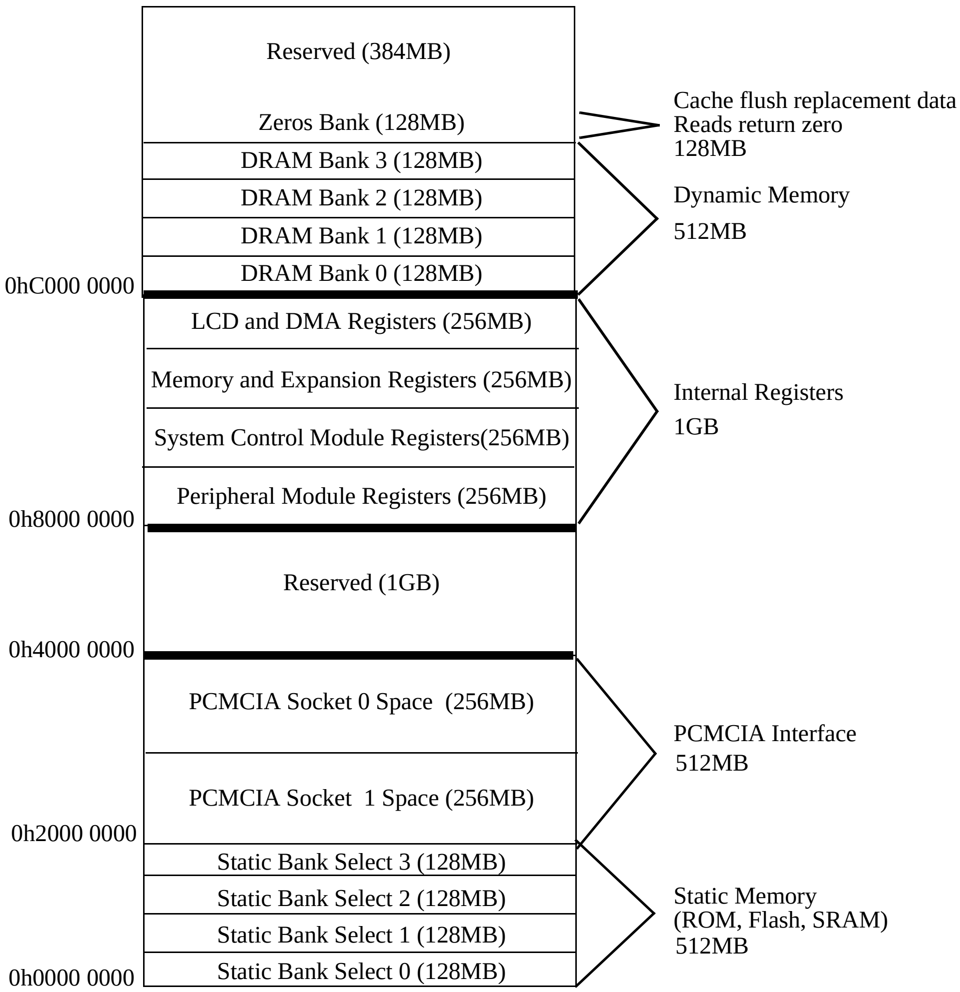

Figure 4 SA-1100 Memory Map

3.0 DC Parameters

This chapter defines the dc parameters for the SA-1100.

3.1 Absolute Maximum Ratings

Table 1 lists the absolute maximum ratings for the SA-1100.

Table 1 SA-1100 DC Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
VDD	Core supply voltage	VSS – 0.5	VSS + 1.65	V	1
VDDX	I/O voltage	MIN(VSS – 0.05, VDD – 0.3)	VSS + 3.6	V	1
Vip	Voltage applied to any pin	VSS – 0.5	VSS + 3.6	V	1
Ts	Storage temperature	– 40	125	°C	1

Note: (1) These are stress SA-1100 ratings only. Exceeding the absolute maximum ratings may permanently damage the device. Operating the device at absolute maximum ratings for extended periods may affect device reliability.

3.2 DC Operating Conditions

Table 2 lists the functional operating dc parameters for the SA-1100.

Table 2 SA-1100 DC Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
Vihc	IC input high voltage	0.8 × VDDX	—	VDDX	V	1, 2
Vilc	IC input low voltage	0.0	—	0.2 × VDDX	V	1, 2
Vohc	OCZ output high voltage	0.8 × VDDX	—	VDDX	V	1, 3
Volc	OCZ output low voltage	0.0	—	0.2 × VDDX	V	1, 3
Iohc	High-level output current	—	—	– 2	mA	—
Iolc	Low-level output current	—	—	2	mA	—
Ta	Ambient operating temperature	– 20	—	70	°C	—
Iin	IC input leakage current	—	10	—	µA	—
Ioh	Output high current (Vout = VDD – 0.4 V)	—	2	—	mA	—
Iol	Output low current (Vout = VSS + 0.4 V)	—	2	—	mA	—
Cin	Input capacitance	—	5	—	pF	—
ESD	HBM model ESD	—	1	—	KV	—

Notes:

(1) Voltages measured with respect to **VSS**.

(2) IC – CMOS-level inputs (includes IC and ICOCZ pin types).

(3) OCZ – Output, CMOS levels, tristatable.

3.3 Power Supply Voltages and Currents

Table 3 specifies the power supply voltages and currents for the SA-1100. For power supply voltages and currents for 2.0-V devices, contact the DIGITAL Semiconductor Customer Technology Center. See Appendix B.

Table 3 SA-1100 Power Supply Voltages and Currents

Parameter	SA-1100 AA	BA	CA	DA	Units
Maximum operating frequency	**133**	**200**	**160**	**220**	**MHz**
Maximum run mode power (total VDD + VDDX)	400	500			mW
Typical idle mode power (total VDD + VDDX)	<50	<65			mW
Maximum sleep mode current (total VDD + VDDX)	50	50			uA
VDD					
Minimum internal power supply voltage	1.35	1.35			V
Nominal internal power supply voltage	1.5	1.5			V
Maximum internal power supply voltage	1.65	1.65			V
VDDX					
Minimum external power supply voltage	3.0	3.0			V
Nominal external power supply voltage	3.3	3.3			V
Maximum external power supply voltage	3.63	3.63			V

4.0 AC Parameters

This chapter defines the ac parameters for the SA-1100.

4.1 Test Conditions

The ac timing diagrams presented in this chapter assume that the outputs of SA-1100 have been loaded with a 50-pF capacitive load on output signals. The output pads of SA-1100 are CMOS drivers that exhibit a propagation delay that increases with the increase in load capacitance. Table 4 lists the output derating figure for each output pad, showing the approximate rate of increase of delay with increasing or decreasing load capacitance for a typical process at room temperature. For derating figures for 2.0-V devices, contact the DIGITAL Semiconductor Customer Technology Center. See Appendix B.

Table 4 SA-1100 Output Derating

Output Signal	Load for Nominal Value	Output Derating (ns/pF) VDD = 1.5 V rising edge	Output Derating (ns/pF) VDD = 1.5 V falling edge	Output Derating (ns/pF) VDD = 2.0 V rising edge	Output Derating (ns/pF) VDD = 2.0 V falling edge
All outputs	50-pF	.086	.077		

4.2 Module Considerations

The edge rates for the SA-1100 processor are such that the lumped load model presented above can only be used for etch lengths up to one inch. Over one inch of etch, the signal is a transmission line and needs to be modeled as such.

4.3 Memory Bus and PCMCIA Signal Timings

During production test, the SA-1100 is placed in testclock bypass mode by the assertion of the **TCKBYP** pin. This mode (not intended for use by customers) bypasses the 3.6864-MHz oscillator and the main PLL and sources the processor clock from the **TESTCLK** pin. During this test mode, all clocks on the SA-1100 are synchronous to **TESTCLK**. In this mode, the basic functionality of the chip is tested and the pin timings relative to **TESTCLK** are measured. The ac parameters are measured in this way for each available processor clock speed and supply voltage at which the device is offered.

The ac specifications for the SA-1100 memory and PCMCIA interfaces are provided relative to the memory clock. In the testclock bypass mode, memory clock is one-half the frequency of **TESTCLK**. Under normal operation, memory clock is one-half the frequency of the processor clock generated by the main PLL.

Even though this clock is not visible to the user, the required pin timing may be inferred through these numbers. Input pins are specified by a required setup and hold to the memory clock. Outputs are specified by a propagation delay from the edge of the memory clock where the drive starts to the time the pin actually transitions. A 50-pF lumped load is assumed to be on each pin. Figure 5 shows the memory bus ac timing definitions and Table 5 describes the ac timing parameters.

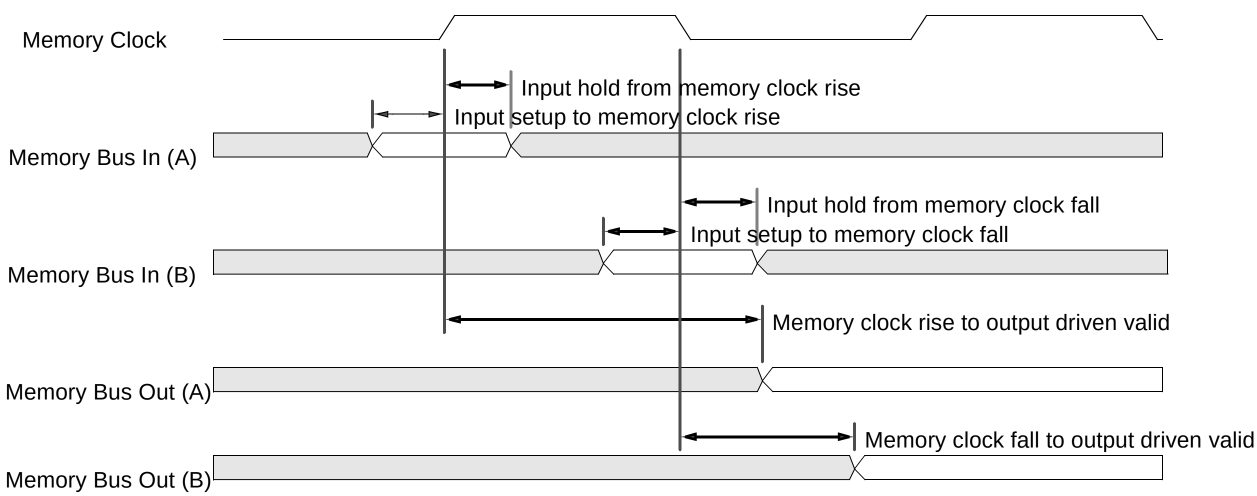

Figure 5 Memory Bus AC Timing Definitions

4.4 LCD Controller Signals

Figure 6 describes the LCD timing parameters. The LCD pin timing specifications are referenced to the pixel clock (L_PCLK).

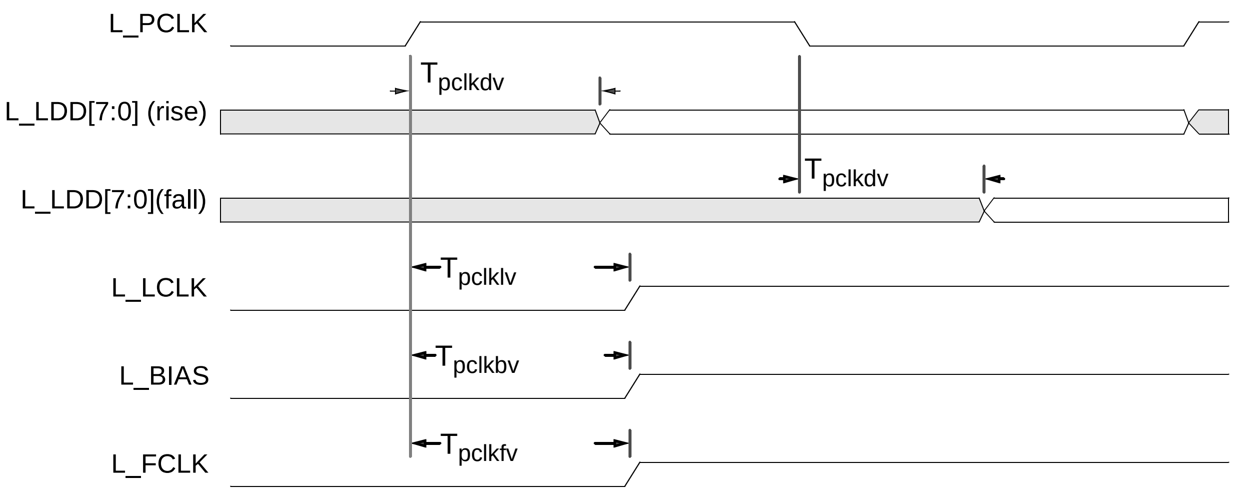

Figure 6 LCD AC Timing Definitions

4.5 MCP Signals

Figure 7 describes the MCP timing parameters. The MCP pin timing specifications are referenced to SCLK_C.

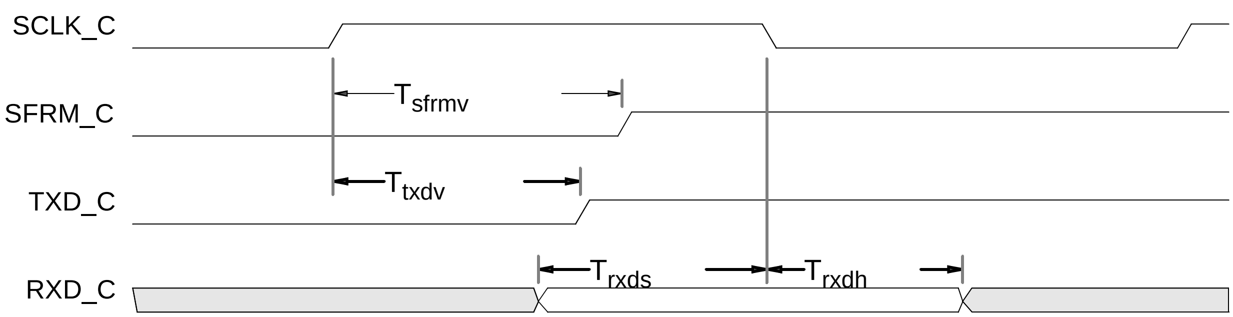

Figure 7 MCP AC Timing Definitions

4.6 Timing Parameters

Table 5 lists the ac timing parameters for the SA-1100 for AA and BA parts. For ac timing parameters for 2.0-V devices, contact the DIGITAL Semiconductor Customer Technology Center. See Appendix B.

Table 5 SA-1100 AC Timing Table for AA and BA Parts

Pin Name	Symbol	Parameter	Min	Max	Unit	Note
Memory Bus						
D[31:0]	Tdfov	Memory clock fall to D[31:0] driven valid	—	10	ns	—
	Tds	D[31:0] valid to memory clock rise/fall (input setup)	0	—	ns	1
	Tdh	Memory clock rise/fall to data invalid (input hold)	4	—	ns	1
nPOE, nPWE, nPIOR, nPIOW, PSKTSEL, nPREG, nPCE[1,2], A[25:0]	Tmfov	Memory clock fall to output driven valid	—	10	ns	5
						—
						—
						—
						—
nIOIS16	Tio16s	nIOIS16 valid to memory clock rise (input setup)	1	—	ns	6
	Tio16h	Memory clock rise to nIOIS16 negated (input hold)	3	—	ns	6
nWE, nOE	Tmrov	Memory clock rise to output driven valid	—	10	ns	—
						—
nRAS[3:0]	Tmrdv	Memory clock rise to output driven valid	—	12	ns	—
nCAS[3:0]	Tcasd	Memory clock rise/fall to nCAS[3:0] driven valid	—	12	ns	2
nCS[3:0]	Tcsd	Memory clock rise to nCS[3:0] driven valid	—	10	ns	—
MCP (CODEC) Interface						
SFRM_C	Tsfrmv	SCLK_C rise to SFRM_C driven valid	—	21	ns	—
RXD_C	Trxds	RXD_C valid to SCLK_C fall (input setup)	0	—	ns	—
	Trxdh	SCLK_C fall to RXD_C invalid (input hold)	4	—	ns	—
TXD_C	Ttxdv	SCLK_C rise to TXD_C valid	—	22	ns	—
LCD Controller						
L_LDD[7:0]	Tpclkdv	L_PCLK rise/fall to L_LDD[7:0] driven valid	—	14	ns	3
L_LCLK	Tpclklv	L_PCLK fall to L_LCLK driven valid	—	14	ns	4
L_FCLK	Tpclkfv	L_PCLK fall to L_FCLK driven valid	—	14	ns	4
L_BIAS	Tpclkbv	L_PCLK rise to L_BIAS driven valid	—	14	ns	4

Notes:
(1) These input pins may be sampled on either the rising or falling edge of the memory clock.
(2) These output pins may be driven on either the rising or falling edge of the memory clock.

(3) The LCD data pins can be programmed to be driven on either the rising or falling edge of the pixel clock (**L_PCLK**).
(4) These LCD signals can, at times, transition when **L_PCLK** is not clocking (between frames). At this time, they are clocked with the internal version of the pixel clock before it is driven out onto the **L_PCLK** pin.
(5) These signals are PCMCIA outputs and are driven by a state machine clocked by BCLK. The user defines BCLK by programming the number of processor clocks per BCLK. Two processor clocks make one memory clock cycle. To ensure proper operation, the user must adhere to the protocol description.
(6) These signals are PCMCIA inputs and are sampled by a state machine clocked by BCLK. The user defines BCLK by programming the number of processor clocks per BCLK. Two processor clocks make one memory clock cycle. To ensure proper operation, the user must adhere to the protocol description.

4.6.1 Asynchronous Signal Timing Descriptions

nPWAIT is an input and is received through a synchronizer. As such, it has no setup and hold specification. The user must adhere to the protocol definition.

When the peripheral pins are in GPIO mode, they are read or written under software control. As outputs, they are driven valid on the pin approximately 20 ns after they are written by software. When inputs, they are received by a synchronizer and must be valid for approximately 20 ns before they are able to be recognized by a CPU read.

nRESET must remain asserted for 150 ms after **VDD** and **VDDX** are stable to properly reset the SA-1100.

nRESET_OUT is asserted for all types of reset (hard, watchdog, sleep, and software) and appears on the pin asynchronously to all clocks.

BATT_FAULT and **VDD_FAULT** are asynchronous inputs and are synchronized to the 32.768-kHz clock after entering the SA-1100. They must be valid for approximately 60 ms before they are recognized by the SA-1100.

PWR_EN asserts when the SA-1100 enters sleep mode and is driven onto the pin following the rising edge of the 32.768-kHz clock. It negates on the same edge as sleep mode is exited.

GP[27:0] are read and written under software control. In addition, an asynchronous edge detect may be performed. When writing a value to these pins, the pin transitions approximately 20 ns after the write is performed. When reading these pins, the signal is first synchronized to the internal memory clock and must be valid for at least 20 ns before it is visible to a processor read. For edge detects, the value on the pin following an edge must be stable for at least 10 ns for the edge to be caught by the edge detect circuit.

UDC+, UDC-, TXD_1, RXD_1, TXD_2, RXD_2, TXD_3, and **RXD_3** are asynchronous relative to any device outside the SA-1100. The output pins, like all outputs on the SA-1100, have been characterized while driving a 50-pF lumped load capacitance.

5.0 Package and Pinout

This chapter describes the SA-1100 pins. Table 6 lists the SA-1100 pins in numeric order, showing the signal type for each pin. All measurements shown in Figure 8 are in millimeters.

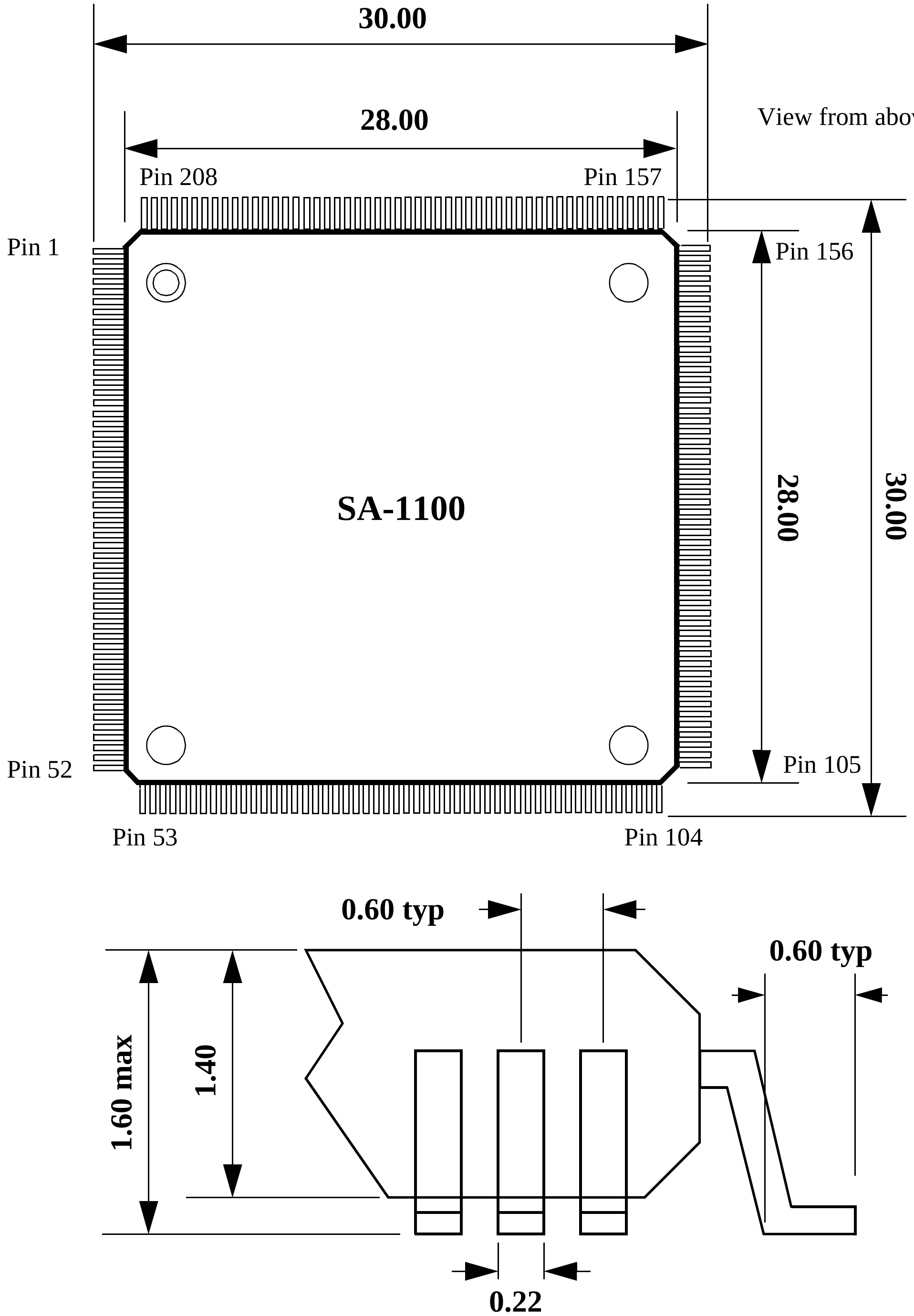

Figure 8 SA-1100 208-Pin LQFP Mechanical Drawing

Table 6 SA-1100 Pinout – 208-Pin Thin Quad Flat Pack

Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type
1	RXD_C	I/O	53	GP[25]	I/O	105	nPIOR	O	157	A[11]	O
2	TXD_C	I/O	54	GP[24]	I/O	106	nPIOW	O	158	A[10]	O
3	**VDDX2**	–	55	GP[23]	I/O	107	**VSSX**	–	159	A[9]	O
4	**VSSX**	–	56	GP[22]	I/O	108	**VDDX2**	–	160	A[8]	O
5	**VDD**	–	57	**VDDX1**	–	109	**VSS**	–	161	**VSSX**	–
6	**VSS**	–	58	**VSSX**	–	110	**VDD**	–	162	**VDDX1**	–
7	D[0]	I/O	59	GP[21]	I/O	111	PSKTSEL	O	163	A[7]	O
8	D[8]	I/O	60	GP[20]	I/O	112	nIOIS16	I	164	A[6]	O
9	D[16]	I/O	61	GP[19]	I/O	113	nPWAIT	I	165	A[5]	O
10	D[24]	I/O	62	GP[18]	I/O	114	nPREG	O	166	A[4]	O
11	D[1]	I/O	63	GP[17]	I/O	115	nPCE2	O	167	A[3]	O
12	D[9]	I/O	64	GP[16]	I/O	116	nPCE1	O	168	A[2]	O
13	D[17]	I/O	65	GP[15]	I/O	117	nWE	O	169	A[1]	O
14	D[25]	I/O	66	GP[14]	I/O	118	nOE	O	170	A[0]	O
15	**VDDX2**	–	67	**VDDX1**	–	119	**VSSX**	–	171	**VSSX**	–
16	**VSSX**	–	68	**VSSX**	–	120	**VDDX2**	–	172	**VDDX1**	–
17	D[2]	I/O	69	GP[13]	I/O	121	nRAS[3]	O	173	UDC-	I/O
18	D[10]	I/O	70	GP[12]	I/O	122	nRAS[2]	O	174	UDC+	I/O
19	D[18]	I/O	71	GP[11]	I/O	123	nRAS[1]	O	175	RXD_1	I/O
20	D[26]	I/O	72	GP[10]	I/O	124	nRAS[0]	O	176	TXD_1	I/O
21	D[3]	I/O	73	GP[9]	I/O	125	nCAS[3]	O	177	RXD_2	I/O
22	D[11]	I/O	74	GP[8]	I/O	126	nCAS[2]	O	178	TXD_2	I/O
23	D[19]	I/O	75	GP[7]	I/O	127	nCAS[1]	O	179	RXD_3	I/O
24	D[27]	I/O	76	GP[6]	I/O	128	nCAS[0]	O	180	TXD_3	I/O
25	**VDD**	–	77	**VDDX1**	–	129	**VSSX**	–	181	**VSSX**	–
26	**VSS**	–	78	**VSSX**	–	130	**VDDX2**	–	182	**VDDX1**	–
27	**VDDX2**	–	79	**VDD**	–	131	**VSS**	–	183	**VSS**	–
28	**VSSX**	–	80	**VSS**	–	132	**VDD**	–	184	TXTAL	I
29	D[4]	I/O	81	GP[5]	I/O	133	nCS[3]	O	185	TEXTAL	O
30	D[12]	I/O	82	GP[4]	I/O	134	nCS[2]	O	186	PEXTAL	O
31	D[20]	I/O	83	GP[3]	I/O	135	nCS[1]	O	187	PXTAL	I
32	D[28]	I/O	84	GP[2]	I/O	136	nCS[0]	O	188	**VDDP**	–
33	D[5]	I/O	85	GP[1]	I/O	137	A[25]	O	189	**VSS**	–
34	D[13]	I/O	86	GP[0]	I/O	138	A[24]	O	190	**VDD**	–
35	D[21]	I/O	87	L_BIAS	I/O	139	A[23]	O	191	nRESET	I
36	D[29]	I/O	88	L_PCLK	I/O	140	A[22]	O	192	nRESET_OUT	O
37	**VDDX2**	–	89	**VDDX1**	–	141	**VSSX**	–	193	**VDDX3**	I
38	**VSSX**	–	90	**VSSX**	–	142	**VDDX2**	–	194	ROMSEL	I
39	D[6]	I/O	91	LDD0	I/O	143	A[21]	O	195	TCK_BYP	I
40	D[14]	I/O	92	LDD1	I/O	144	A[20]	O	196	TESTCLK	I
41	D[22]	I/O	93	LDD2	I/O	145	A[19]	O	197	TMS	I
42	D[30]	I/O	94	LDD3	I/O	146	A[18]	O	198	TCK	I
43	D[7]	I/O	95	LDD4	I/O	147	A[17]	O	199	TDI	I
44	D[15]	I/O	96	LDD5	I/O	148	A[16]	O	200	TDO	O
45	D[23]	I/O	97	LDD6	I/O	149	A[15]	O	201	nTRST	I
46	D[31]	I/O	98	LDD7	I/O	150	A[14]	O	202	BATT_FAULT	I
47	**VDD**	–	99	**VDDX1**	–	151	**VSS**	–	203	**VSSX**	–
48	**VSS**	–	100	**VSSX**	–	152	**VDD**	–	204	**VDDX1**	–
49	**VDDX2**	–	101	L_LCLK	I/O	153	**VSSX**	–	205	VDD_FAULT	I
50	**VSSX**	–	102	L_FCLK	I/O	154	**VDDX2**	–	206	PWR_EN	O
51	GP[27]	I/O	103	nPOE	O	155	A[13]	O	207	SFRM_C	O
52	GP[26]	I/O	104	nPWE	O	156	A[12]	O	208	SCLK_C	O

Note: All **VDDX1**, **VDDX2**, and **VDDX3** pins should be connected directly to the **VDDX** power plane of the system board. **VDDP** should be connected directly to the **VDD** plane of the system board.

A Register Summary

This appendix describes all of the SA-1100 internal registers.

Physical Address	Symbol	Register Name
GPIO registers		
0h 9004 0000	GPLR	GPIO pin level register.
0h 9004 0004	GPDR	GPIO pin direction register.
0h 9004 0008	GPSR	GPIO pin output set register.
0h 9004 000C	GPCR	GPIO pin output clear register.
0h 9004 0010	GRER	GPIO rising-edge register.
0h 9004 0014	GFER	GPIO falling-edge register.
0h 9004 0018	GEDR	GPIO edge detect status register.
0h 9004 001C	GAFR	GPIO alternate function register.
Interrupt Controller Registers		
0h 9005 0000	ICIP	Interrupt controller irq pending register.
0h 9005 0004	ICMR	Interrupt controller mask register.
0h 9005 0008	ICLR	Interrupt controller FIQ level register.
0h 9005 0010	ICFP	Interrupt controller FIQ pending register.
0h 9005 0020	ICPR	Interrupt controller pending register.
0h 9005 000c	ICPR	Interrupt controller control register.
Real-Time Clock Registers		
0h 9001 0004	RCNR	Real-time clock count register.
0h 9001 0000	RTAR	Real-time clock alarm register.
0h 9001 0010	RTSR	Real-time clock status register.
0h 9001 0008	RTTR	Real-time clock trim register.

Physical Address	Symbol	Register Name
OS Timer Registers		
0h 9000 0000	OSMR[0]	OS timer match registers[3:0].
0h 9000 0004	OSMR[1]	
0h 9000 0008	OSMR[2]	
0h 9000 000C	OSMR[3]	
0h 9000 0010	OSCR	OS timer counter register.
0h 9000 0014	OSSR	OS timer status register.
0h 9000 0018	OWER	OS timer watchdog enable register.
0h 9000 001C	OIER	OS timer interrupt enable register.
Power Manager Registers		
0h 9002 0000	PMCR	Power manager control register.
0h 9002 0004	PSSR	Power manager sleep status register.
0h 9002 0008	PSPR	Power manager scratchpad register.
0h 9002 000C	PWER	Power manager wakeup enable register.
0h 9002 0010	PCFR	Power manager configuration register.
0h 9002 0014	PPCR	Power manager PLL configuration register.
0h 9002 0018	PGSR	Power manager GPIO sleep state register.
0h 9002 001C	POSR	Power manager oscillator status register.
Reset Controller Registers		
0h 9003 0000	RSRR	Reset controller software reset register.
0h 9003 0004	RCSR	Reset controller status register.
0h 9003 0008	TUCR	Reserved for test.
Memory Controller Registers		
0xA000 0000	MDCNFG	DRAM configuration register.
0xA000 0004	MDCAS0	DRAM CAS waveform shift register 0.
0xA000 0008	MDCAS1	DRAM CAS waveform shift register 1.
0xA000 000C	MDCAS2	DRAM CAS waveform shift register 2.
0xA000 0010	MSC0	Static memory control register 0.

Physical Address	Symbol	Register Name
0xA000 0014	MSC1	Static memory control register 1.
0xA000 0018	MECR	Expansion bus configuration register.
DMA Controller Registers		
0h B000 0000	DDAR0	DMA device address register.
0h B000 0004	DCSR0	DMA control/status register 0 – write ones to set.
0h B000 0008		Write ones to clear.
0h B000 000C		Read only.
0h B000 0010	DBSA0	DMA buffer A start address 0.
0h B000 0014	DBTA0	DMA buffer A transfer count 0.
0h B000 0018	DBSB0	DMA buffer B start address 0.
0h B000 001C	DBTB0	DMA buffer B transfer count 0.
0h B000 0020	DDAR1	DMA device address register 1.
0h B000 0024	DCSR1	DMA control/status register 1 – write ones to set.
0h B000 0028		Write ones to clear.
0h B000 002C		Read only.
0h B000 0030	DBSA1	DMA buffer A start address 1.
0h B000 0034	DBTA1	DMA buffer A transfer count 1.
0h B000 0038	DBSB1	DMA buffer B start address 1.
0h B000 003C	DBTB1	DMA buffer B transfer count 1.
0h B000 0040	DDAR2	DMA device address register 2.
0h B000 0044	DCSR2	DMA control/status register 2 – write ones to set.
0h B000 0048		Write ones to clear.
0h B000 004C		Read only.
0h B000 0050	DBSA2	DMA buffer A start address 2.
0h B000 0054	DBTA2	DMA buffer A transfer count 2.
0h B000 0058	DBSB2	DMA buffer B start address 2.
0h B000 005C	DBTB2	DMA buffer B transfer count 2.

Physical Address	Symbol	Register Name
0h B000 0060	DDAR3	DMA device address register 3.
0h B000 0064	DCSR3	DMA control/status register 3 – write ones to set.
0h B000 0068		Write ones to clear.
0h B000 006C		Read only.
0h B000 0070	DBSA3	DMA buffer A start address 3.
0h B000 0074	DBTA3	DMA buffer A transfer count 3.
0h B000 0078	DBSB3	DMA buffer B start address 3.
0h B000 007C	DBTB3	DMA buffer B transfer count 3.
0h B000 0080	DDAR4	DMA device address register 4.
0h B000 0084	DCSR4	DMA control/status register 4 – write ones to set.
0h B000 0088		Write ones to clear.
0h B000 008C		Read only.
0h B000 0090	DBSA4	DMA buffer A start address 4.
0h B000 0094	DBTA4	DMA buffer A transfer count 4.
0h B000 0098	DBSB4	DMA buffer B start address 4.
0h B000 009C	DBTB4	DMA buffer B transfer count 4.
0h B000 00A0	DDAR5	DMA device address register 5.
0h B000 00A4	DCSR5	DMA control/status register 5 – write ones to set.
0h B000 00A8		Write ones to clear.
0h B000 00AC		Read only.
0h B000 00B0	DBSA5	DMA buffer A start address 5.
0h B000 00B4	DBTA5	DMA buffer A transfer count 5.
0h B000 00B8	DBSB5	DMA buffer B start address 5.
0h B000 00BC	DBTB5	DMA buffer B transfer count 5.
LCD Controller Registers		
0hB010 0000	LCCR0	LCD controller control register 0.
0hB010 0004	LCSR	LCD controller status register.

Physical Address	Symbol	Register Name
0hB010 0008 – 0hB010 000C	—	Reserved.
0hB010 0010	DBAR1	DMA channel 1 base address register.
0hB010 0014	DCAR1	DMA channel 1 current address register.
0hB010 0018	DBAR2	DMA channel 2 base address register.
0hB010 001C	DCAR2	DMA channel 2 current address register.
0hB010 0020	LCCR1	LCD controller control register 1.
0hB010 0024	LCCR2	LCD controller control register 2.
0hB010 0028	LCCR3	LCD controller control register 3.
0hB010 002C – 0hB010 FFFF	—	Reserved.
UDC Registers (Serial Port 0)		
0h8000 0000	UDCCR	UDC control register.
0h8000 0004	UDCAR	UDC address register.
0h8000 0008	UCDOMP	UDC OUT max packet register.
0h8000 000C	UDCIMP	UDC IN max packet register.
0h8000 0010	UDCCS0	UDC endpoint 0 control/status register.
0h8000 0014	UDCCS1	UDC endpoint 1 (out) control/status register.
0h8000 0018	UDCCS2	UDC endpoint 2 (in) control/status register.
0h8000 001C	UDCD0	UDC endpoint 0 data register.
0h8000 0020	UDCWC	UDC endpoint 0 write count register.
0h8000 0024	—	Reserved.
0h8000 0028	UDCDR	UDC transmit/receive data register (FIFOs).
0h8000 002C	—	Reserved.
0h8000 0030	UDCSR	UDC status/interrupt register.
UART Registers (Serial Port 1)		
0h 8001 0000	UTCR0	UART control register 0.
0h 8001 0004	UTCR1	UART control register 1.
0h 8001 0008	UTCR2	UART control register 2.

Physical Address	Symbol	Register Name
0h 8001 000C	UTCR3	UART control register 3.
0h 8001 0010	—	Reserved.
0h 8001 0014	UTDR	UART data register.
0h 8001 0018	—	Reserved.
0h 8001 001C	UTSR0	UART status register 0.
0h 8001 0020	UTSR1	UART status register 1.
0h 8001 0024 – 0h 8001 FFFF	—	Reserved.
SDLC Registers (Serial Port 1)		
0h 8002 0060	SDCR0	SDLC control register 0.
0h 8002 0064	SDCR1	SDLC control register 1.
0h 8002 0068	SDCR2	SDLC control register 2.
0h 8002 006C	SDCR3	SDLC control register 3.
0h 8002 0070	SDCR4	SDLC control register 4.
0h 8002 0074	—	Reserved.
0h 8002 0078	SDDR	SDLC data register.
0h 8002 007C	—	Reserved.
0h 8002 0080	SDSR0	SDLC status register 0.
0h 8002 0084	SDSR1	SDLC status register 1.
0h 8002 0088 – 0h 8002 FFFF	—	Reserved.
ICP – UART Registers (Serial Port 2)		
0h 8003 0000	UTCR0	UART control register 0.
0h 8003 0004	UTCR1	UART control register 1.
0h 8031 0008	UTCR2	UART control register 2.
0h 8003 000C	UTCR3	UART control register 3.
0h 8003 0010	UTCR4	UART control register 4.
0h 8003 0014	UTDR	UART data register.
0h 8003 0018	—	Reserved.

Physical Address	Symbol	Register Name
0h 8003 001C	UTSR0	UART status register 0.
0h 8003 0020	UTSR1	UART status register 1.
0h 8003 0024 – 0h 8003 FFFF	—	Reserved.
ICP – HSSP Registers (Serial Port 2)		
0h 8004 0060	HSCR0	HSSP control register 0.
0h 8004 0064	HSCR1	HSSP control register 1.
0h 8004 0068	—	Reserved.
0h 8004 006C	HSDR	HSSP data register.
0h 8004 0070	—	Reserved.
0h 8004 0074	HSSR0	HSSP status register 0.
0h 8004 0078	HSSR1	HSSP status register 1.
0h 8004 007C – 0h 8004 FFFF	—	Reserved.
UART Registers (Serial Port 3)		
0h 8005 0000	UTCR0	UART control register 0.
0h 8005 0004	UTCR1	UART control register 1.
0h 8005 0008	UTCR2	UART control register 2.
0h 8005 000C	UTCR3	UART control register 3.
0h 8005 0010	—	Reserved.
0h 8005 0014	UTDR	UART data register.
0h 8005 0018	—	Reserved.
0h 8005 001C	UTSR0	UART status register 0.
0h 8005 0020	UTSR1	UART status register 1.
0h 8005 0024 – 0h 8005 FFFF	—	Reserved.
MCP Registers (Serial Port 4)		
0h 8006 0000	MCCR0	MCP control register 0.
0h 8006 0004	—	Reserved.

Physical Address	Symbol	Register Name
0h 8006 0008	MCDR0	MCP data register 0.
0h 8006 000C	MCDR1	MCP data register 1.
0h 8006 0010	MCDR2	MCP data register 2.
0h 8006 0014	—	Reserved.
0h 8006 0018	MCSR	MCP status register.
0h 8006 001C – 0h 8006 005C	—	Reserved.
SSP Registers (Serial Port 4)		
0h 8007 0060	SSCR0	SSP control register 0.
0h 8007 0064	SSCR1	SSP control register 1.
0h 8007 0068	—	Reserved.
0h 8007 006C	SSDR	SSP data register.
0h 8007 0070	—	Reserved.
0h 8007 0074	SSSR	SSP status register.
0h 8007 0078 – 0h 8007 FFFF	—	Reserved.
PPC Registers		
0h 9006 0000	PPDR	PPC pin direction register.
0h 9006 0004	PPSR	PPC pin state register.
0h 9006 0008	PPAR	PPC pin assignment register.
0h 9006 000C	PSDR	PPC sleep mode direction register.
0h 9006 0010	PPFR	PPC pin flag register.
0h 9006 0030	MCCR1	MCP control register 1.
0h 9006 0034 – 0h 9006 FFFF	—	Reserved.

B Support, Products, and Documentation

If you need technical support, a *DIGITAL Semiconductor Product Catalog*, or help deciding which documentation best meets your needs, visit the DIGITAL Semiconductor World Wide Web Internet site:

http://www.digital.com/semiconductor

You can also contact the DIGITAL Semiconductor Information Line or the DIGITAL Semiconductor Customer Technology Center for support.

For documentation and general information:	
DIGITAL Semiconductor Information Line	
United States and Canada:	1–800–332–2717
Outside North America:	1–510–490–4753
Electronic mail address:	semiconductor@digital.com

For technical support:	
DIGITAL Semiconductor Customer Technology Center	
Phone (U.S. and international):	1–978–568–7474
Fax:	1–978–568–6698
Electronic mail address:	ctc@hlo.mts.dec.com

Support, Products, and Documentation

DIGITAL Semiconductor Products

To order the DIGITAL Semiconductor SA-1100 Microprocessor, contact your local distributor. The following tables list some of the semiconductor products available from DIGITAL Semiconductor.

Note: The following products and order numbers might have been revised. For the latest versions, contact your local distributor.

Products	Order Number
DIGITAL Semiconductor SA-1100 Microprocessor (133 MHz)	DE–S1100–AA
DIGITAL Semiconductor SA-1100 Microprocessor (200 MHz)	DE–S1100–BA
DIGITAL Semiconductor SA-1100 Microprocessor (166 MHz)	DE–S1100–CA
DIGITAL Semiconductor SA-1100 Microprocessor (220 MHz)	DE–S1100–DA
ARM Software Developer’s Kit – End User License	QR–21B81–01
ARM Software Developer’s Kit – Site License	QR–21B81–02

Evaluation board kits include an evaluation board, and can include a complete design kit, an installation kit, or an accessories kit.

Evaluation Board Kits	Order Number
DIGITAL Semiconductor SA-1100 Microprocessor Evaluation Platform	DE–1S110–0A

DIGITAL Semiconductor Documentation

The following table lists some of the available DIGITAL Semiconductor documentation.

Title	Order Number
DIGITAL Semiconductor SA-1100 Microprocessor for Portable Applications Product Brief	EC–R59EB–TE
DIGITAL Semiconductor SA-1100 Microprocessor for Embedded Applications Product Brief	EC–R8XTB–TE
DIGITAL Semiconductor SA-1100 Microprocessor Technical Reference Manual	EC–R5MTB–TE
DIGITAL Semiconductor SA-1100 Microprocessor Evaluation Platform Product Brief	EC–R8BEA–TE
DIGITAL Semiconductor SA-1100 Microprocessor Evaluation Platform User’s Guide	EC–R7MWB–TE

Third–Party Documentation

You can order the following third-party documentation directly from the vendor.

Title	Vendor
IEEE Standard 1149.1 – 1990, Standard Test Access Port and Boundary-Scan Architecture	The Institute of Electrical and Electronics Engineers, Inc. U.S. 1–800–701–4333 International 1–908–981–0060 Fax 1–908–981–9667