

DATA SHEET

PHN110

N-channel enhancement mode
MOS transistor

Product specification
Supersedes data of November 1994
File under Discrete Semiconductors, SC07

1996 Apr 02

N-channel enhancement mode MOS transistor

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FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectifying.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

N-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

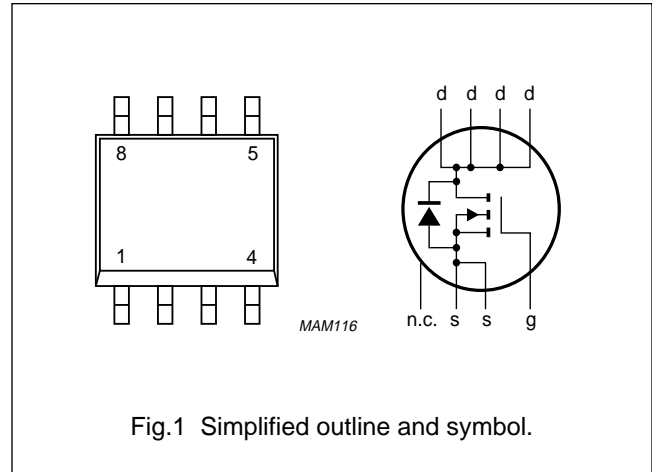


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	$I_S = 1.25$ A	–	1.2	V
V_{GS}	gate-source voltage (DC)		–	± 20	V
V_{GSth}	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)	$T_s = 80$ °C	–	4	A
R_{DSon}	drain-source on-state resistance	$I_D = 2.2$ A; $V_{GS} = 10$ V	–	0.1	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	2.8	W

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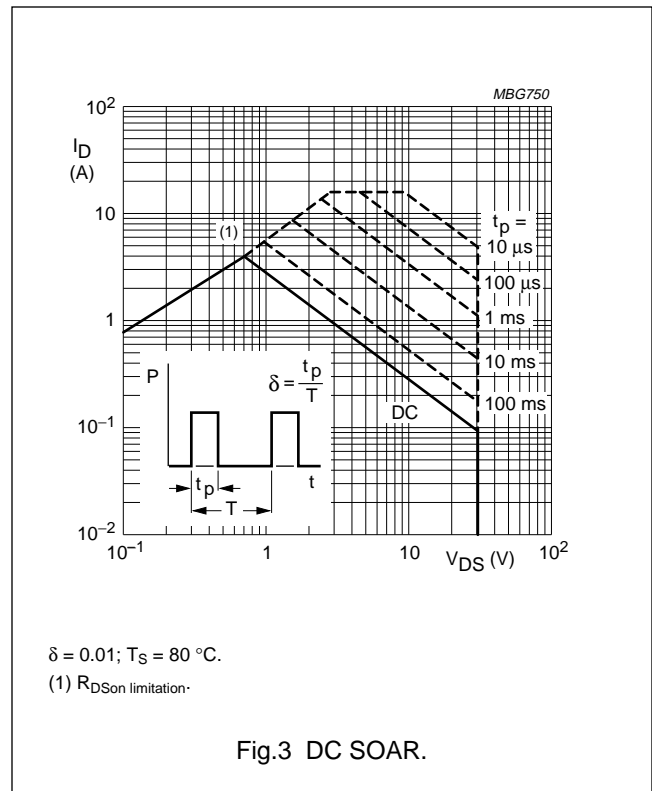
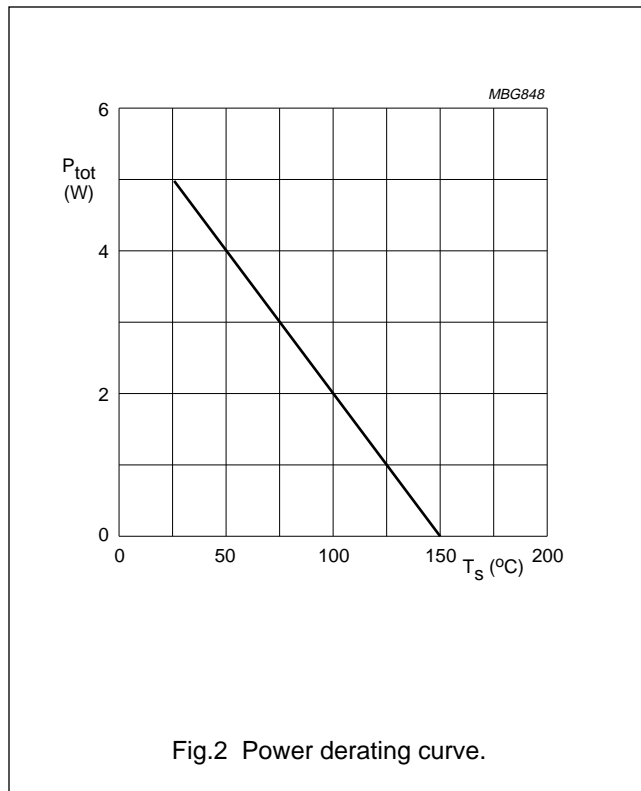
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	$T_s = 80\text{ °C}$; note 1	–	4	A
I_{DM}	peak drain current	note 2	–	16	A
P_{tot}	total power dissipation	$T_s = 80\text{ °C}$	–	2.8	W
		$T_{amb} = 25\text{ °C}$; note 3	–	2.4	W
		$T_{amb} = 25\text{ °C}$; note 4	–	1.1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	$T_s = 80\text{ °C}$	–	3.5	A
I_{SM}	peak pulsed source current	note 2	–	14	A

Notes

- T_s is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Value based on PCB with a $R_{th\ a-tp}$ (ambient to tie-point) of 27.5 K/W.
- Value based on PCB with a $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	25	K/W

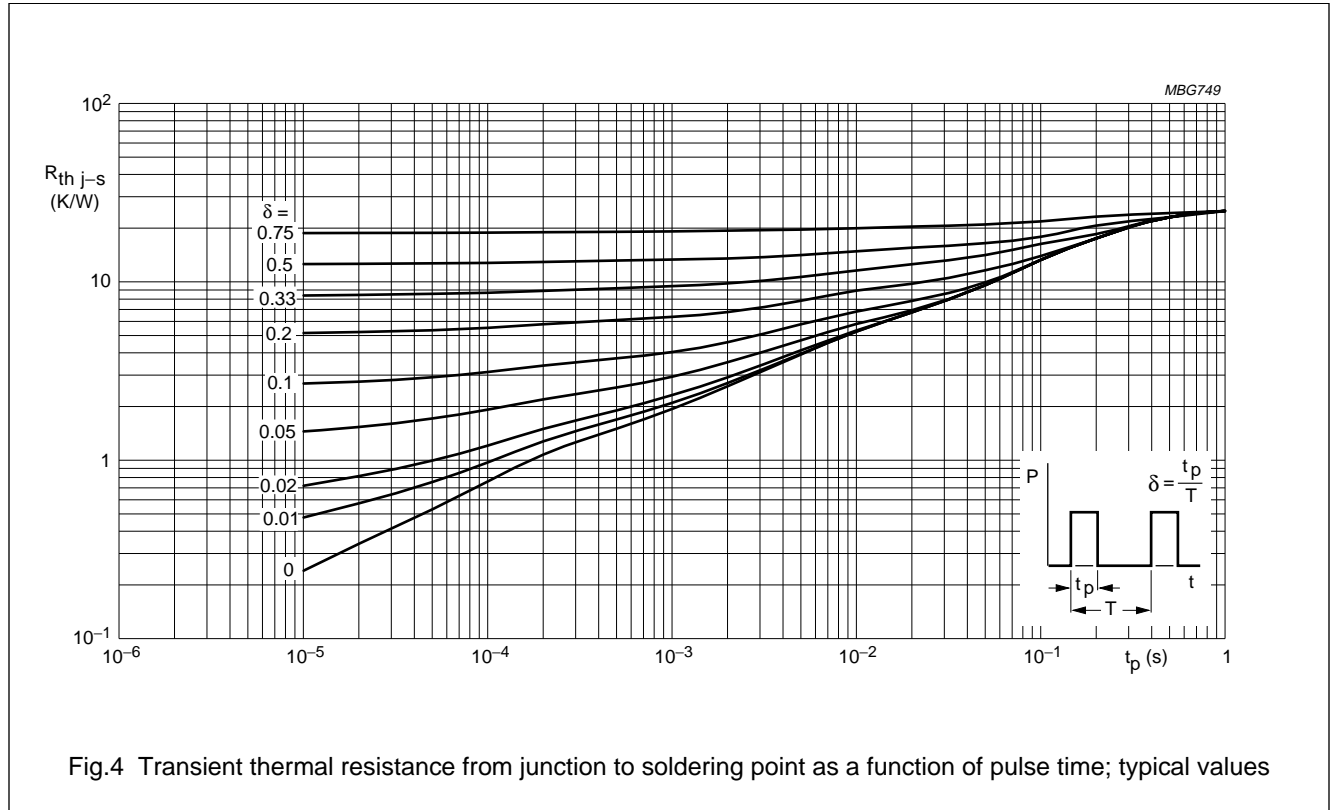


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values

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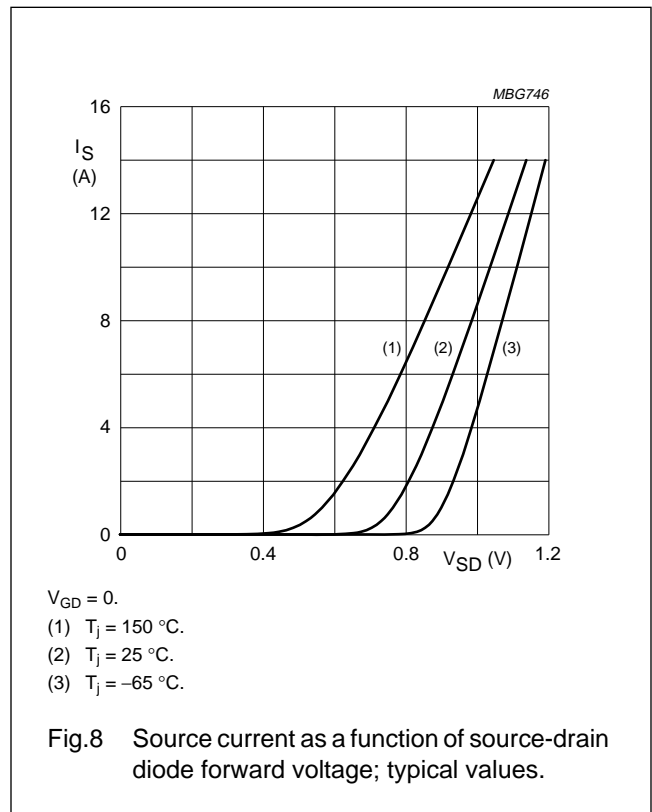
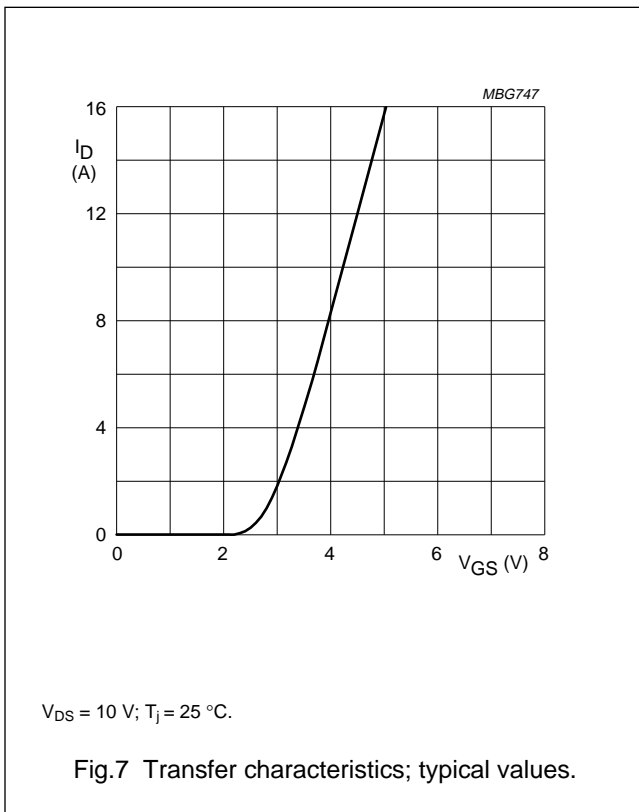
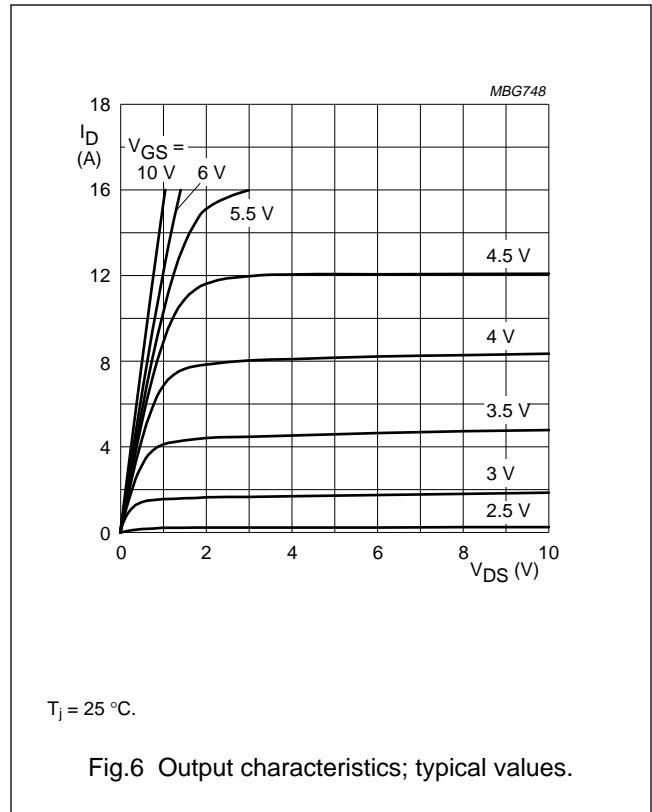
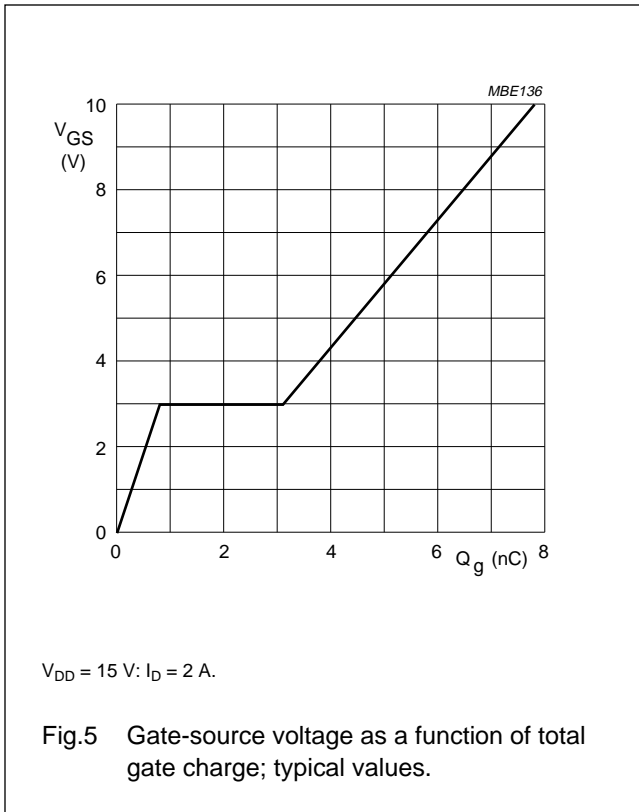
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CHARACTERISTICS $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 10\ \mu\text{A}$	30	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = 1\ \text{mA}$	1	–	2.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 24\ \text{V}$	–	–	100	nA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	–	–	± 100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}; I_D = 1\ \text{A}$	–	0.11	0.2	Ω
		$V_{GS} = 10\ \text{V}; I_D = 2\ \text{A}$	–	0.08	0.1	Ω
C_{iss}	input capacitance	$V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$	–	250	–	pF
C_{oss}	output capacitance	$V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$	–	140	–	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$	–	50	–	pF
Q_g	total gate charge	$V_{GS} = 10\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 2\ \text{A}$	–	10	30	nC
Q_{gs}	gate-source charge	$V_{GS} = 10\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 2\ \text{A}$	–	1	–	nC
Q_{gd}	gate-drain charge	$V_{GS} = 10\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 2\ \text{A}$	–	2.5	–	nC
Switching times (see Fig 11)						
$t_{d(on)}$	turn-on delay time	$V_{GS} = 0\ \text{to}\ 10\ \text{V}; V_{DD} = 15\ \text{V};$ $I_D = 1\ \text{A}; R_L = 15\ \Omega; R_{gen} = 6\ \Omega$	–	4.5	–	ns
t_f	fall time		–	3.5	–	ns
t_{on}	turn-on switching time		–	8	16	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = 10\ \text{to}\ 0\ \text{V}; V_{DD} = 15\ \text{V};$ $I_D = 1\ \text{A}; R_L = 15\ \Omega; R_{gen} = 6\ \Omega$	–	15	–	ns
t_r	rise time		–	10	–	ns
t_{off}	turn-off switching time		–	25	50	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	$V_{GS} = 0; I_S = 1.25\ \text{A}$	–	–	1.2	V
t_{rr}	reverse recovery time	$I_S = 1.25\ \text{A}; di/dt = -100\ \text{A}/\mu\text{s}$	–	35	100	ns

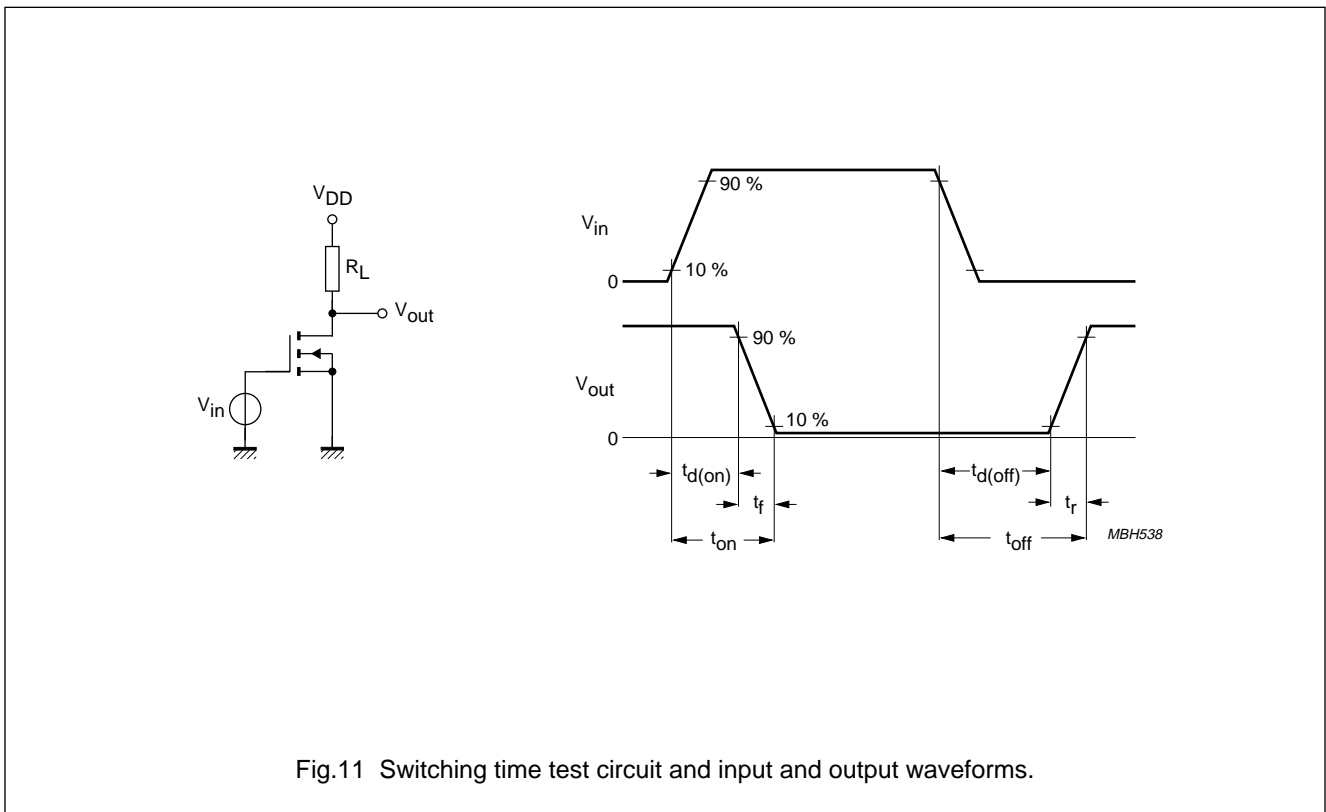
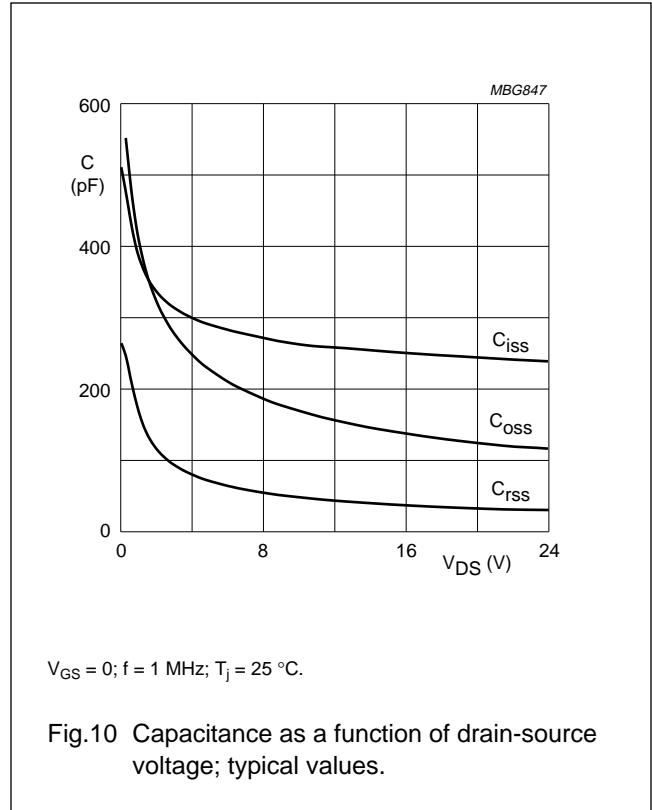
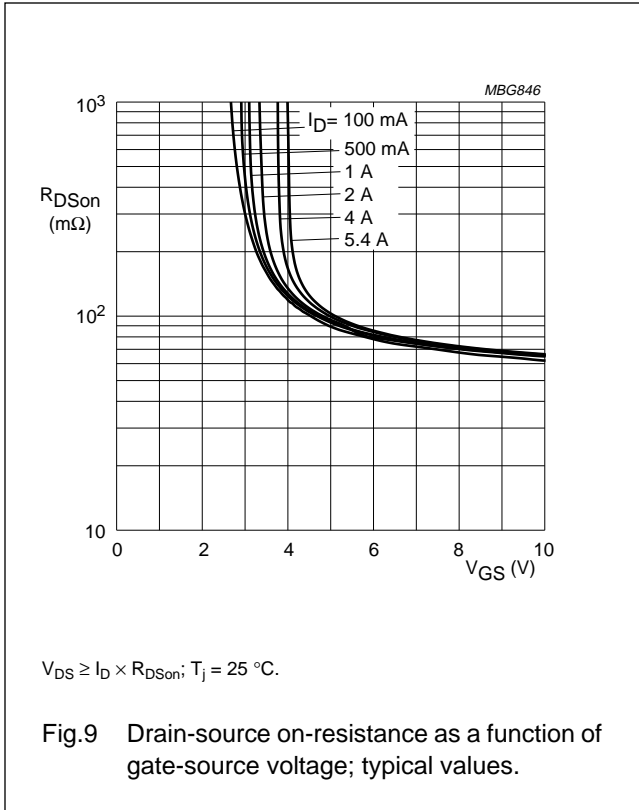
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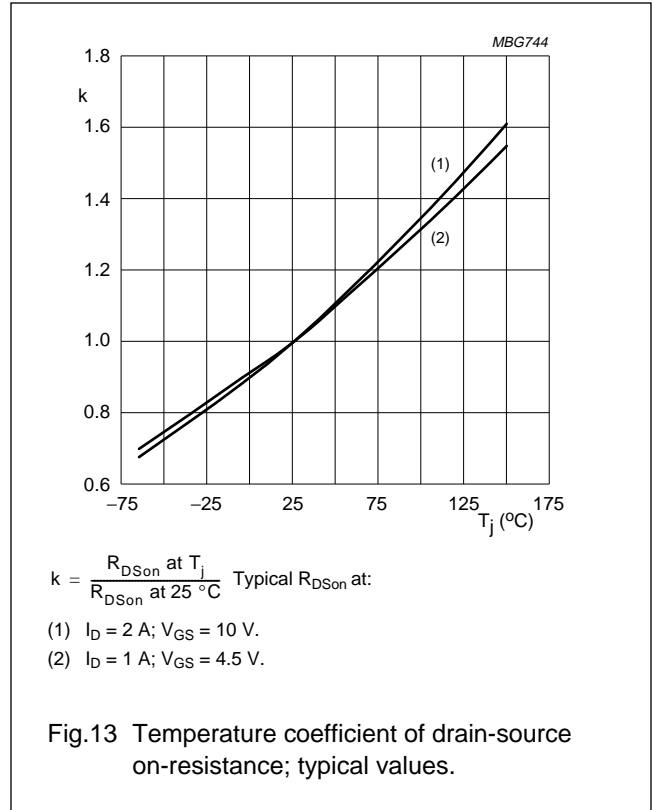
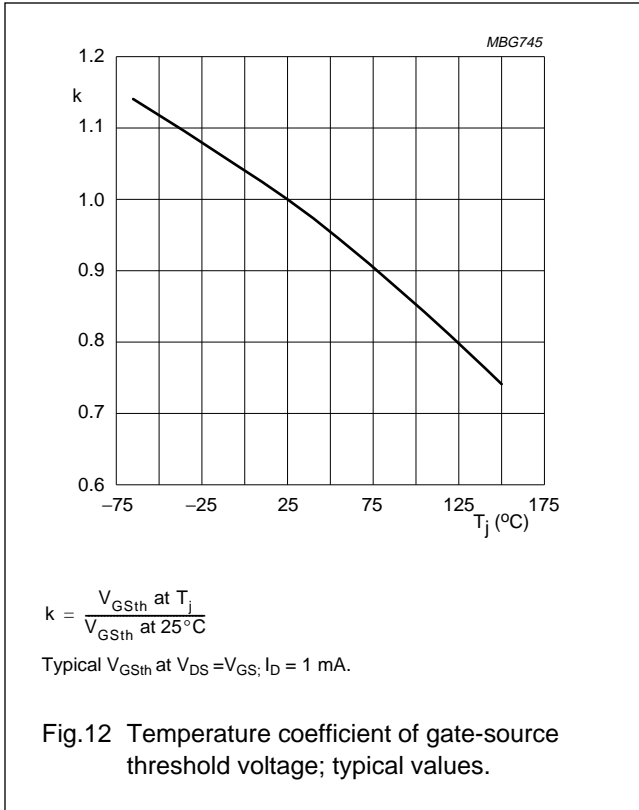
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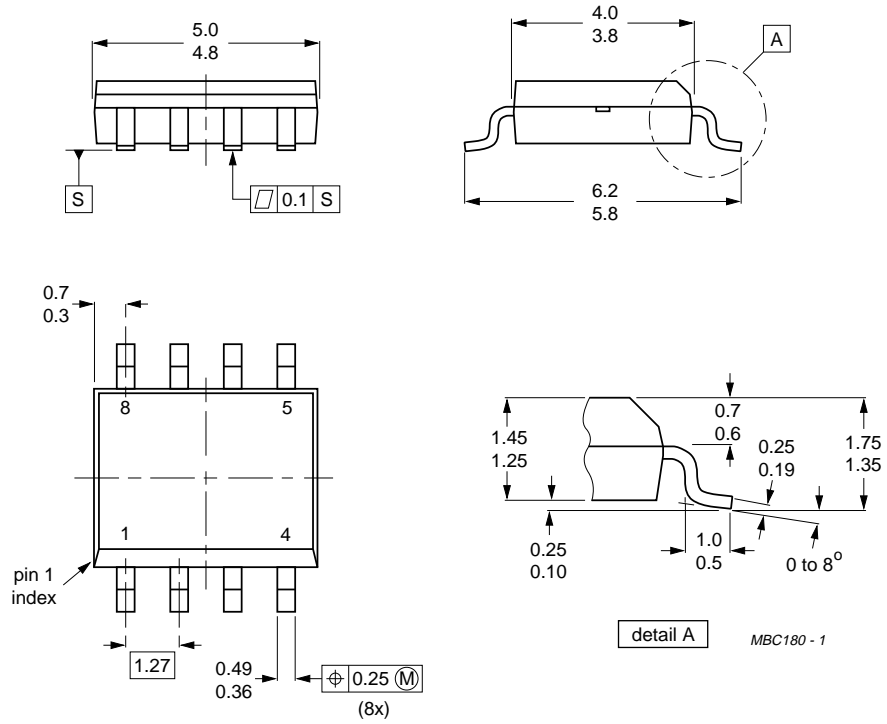
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PACKAGE OUTLINE



Dimensions in mm.

Fig.14 Plastic small outline package; 8 leads; body width 3.9 mm; SO8 (SOT96-1).

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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